DATA HANDBOOK

ABT
MULTIBYTE™ Advanced BiCMOS Bus Interface Logic

BOOK IC23 1991

Philips Semiconductors

PHILIPS

ABT MULTIBYTE™ ADVANCED BiCMOS INTERFACE BUS LOGIC

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Signetics registers eligible circuits under
the Semiconductor Chip Protection Act.

Preface

Signetics would like to thank you for your interest in our products.

This handbook is meant to replace our 1990 *ABT Advanced BiCMOS Interface Logic* data manual. It contains full Product Specifications for some parts covered by Preliminary data in the previous manual. In addition, there are Product or Preliminary Specifications on many new ABT or MB interface products. The MB2000 and MB4000 series are composed of two and four byte wide versions of the most used interface components. These devices offer you all the benefits of QUBiC, our truly integrated BiCMOS process. Using our fastest bipolar modules, combined with a sub-micron CMOS you get high performance: very high speed, plus low, low power, plus high output drive, plus excellent noise immunity, are now combined with the space-saving advantages of "multiple byte" configurations in a single package.

Congratulations on making the right selection for your 1990's design needs.

Advanced BiCMOS Products

Product Status

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains a preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible products.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Section 1
General Information

INDEX

Alphanumeric Index

74ABTXXX FAMILY

Alphanumeric Index

MBXXXX FAMILY

Functional Index

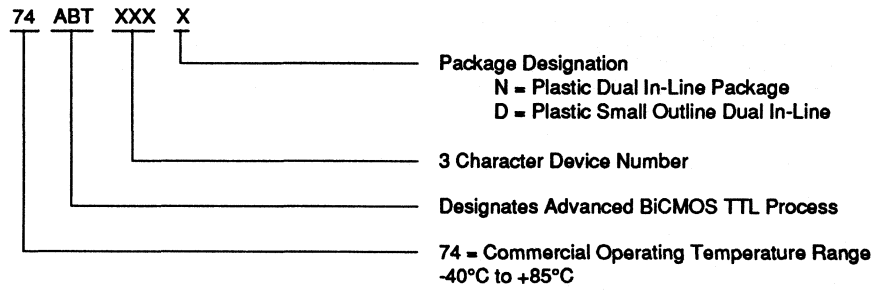
74ABTXXX FAMILY

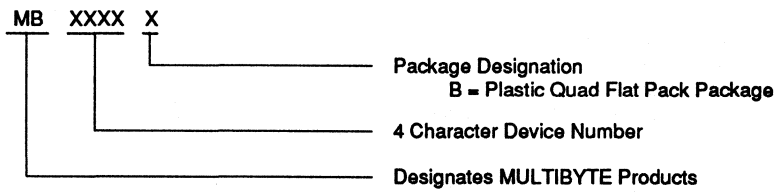
Functional Index

Functional Index

MBXXXX FAMILY

Ordering Information





TEMPERATURE RANGE	DEVICE NUMBER	PACKAGE STYLE
T_{amb} = -40°C to +85°C	74ABTXXX	D = Plastic Small Outline N = Plastic Dual In-Line
	MBXXXX	B = Plastic Quad Flat Pack

Section 2
Introduction

INDEX

Introduction to ABT and MULTIBYTE

INTRODUCTION

A true BICMOS process, such as QUBiC, gives an integrated circuit designer a great deal of freedom in approaching the optimum requirement goals of the system designer. The input and output structures can be designed in such a way that they are optimum from a system standpoint. Noise characteristics such as ground bounce and EMI can be minimized without performance degradation. Speed can be maximized towards that of the fastest bipolar devices and power dissipation can be greatly reduced below even pure CMOS approaches.

QUBIC PROCESS

The QUBiC BiCMOS process from Signetics is truly a major achievement in semiconductor process technology. With equal emphasis on optimization of the CMOS as well as the bipolar devices, the process offers 13GHz bipolar NPN devices, one micron NMOS devices, and one micron PMOS devices, altogether with three layers of Al/Cu interconnect. The devices are completely free of latch–up, have high ESD protection, show no electromigration, and, due to low bipolar reverse leakage currents and lightly doped CMOS drains, show extremely long reliability lifetimes. From an electrical performance standpoint, the results of this process are clear.

AC CHARACTERISTICS

Speed is almost always the first characteristic considered when choosing an integrated circuit. With bus frequencies constantly on the rise and the demand for greater data transfer rates continuously increasing, bus interface devices have become especially sensitive to speed. Figure 1 clearly shows the advantage of Signetics ABT Advanced BiCMOS interface devices.

Supply voltage and temperature stability is also an important feature of a product. Figure 1 shows the propagation delay versus change in the supply voltage and change in temperature. The temperature stability of ABT and MULTIBYTE devices is again a by–product of the process technology. A bipolar transistor generally becomes faster with increases in temperature and a CMOS transistor slows down with an increase in temperature. The effective addition of these two phenomena create the desirable feature shown in the figure. The flat slope of these curves essentially removes the variables of power supply and temperature from a designer's list of considerations. It also ensures that the device will be more resistant to unexpected system deviations from supply and temperature norms.

INPUT CHARACTERISTICS

The ABT Advanced BiCMOS and MULTIBYTE bus interface devices have TTL input electrical levels, guaranteed switching between 0.8V and 2.0V (typically 1.6V) in order to be driven by TTL or CMOS level buses. They have the desired CMOS characteristic of very low input current loading and input capacitance in the 3 – 4pF range. This feature ensures that the devices lightly load the buses they are interfacing to, allowing the devices to be driven from lower output current devices on a local bus, thus allowing higher system integration.

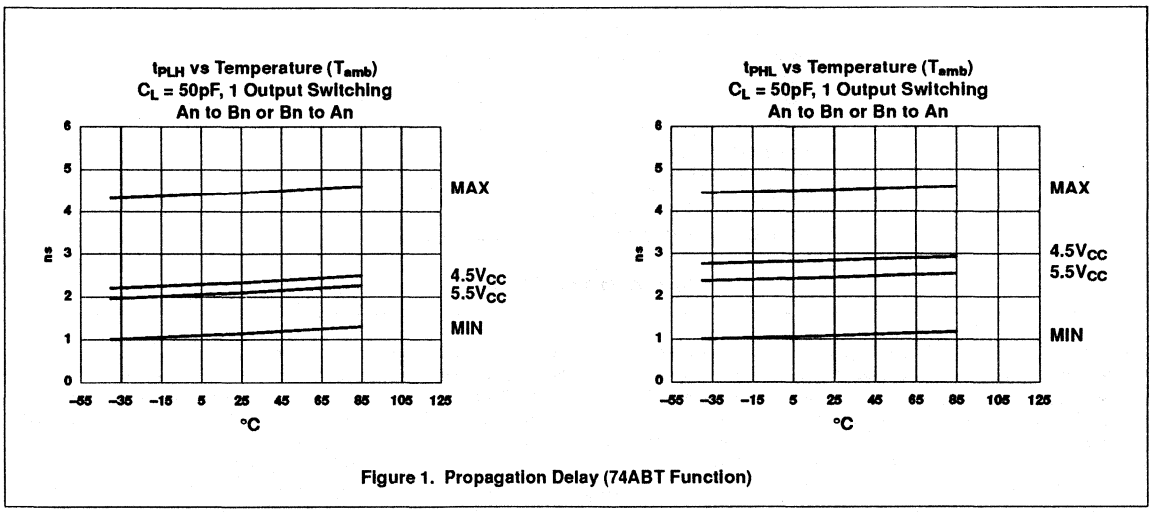
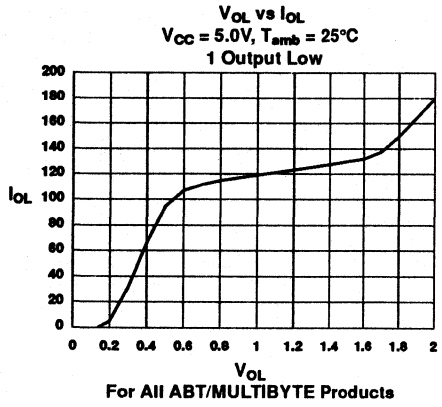
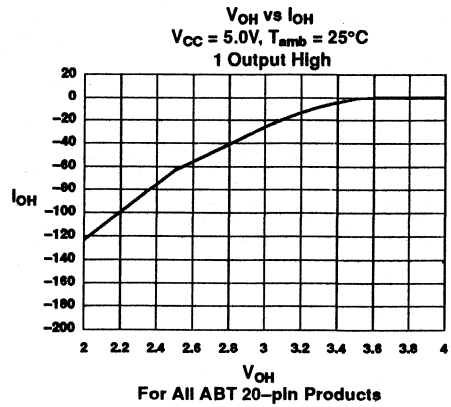


Figure 1. Propagation Delay (74ABT Function)

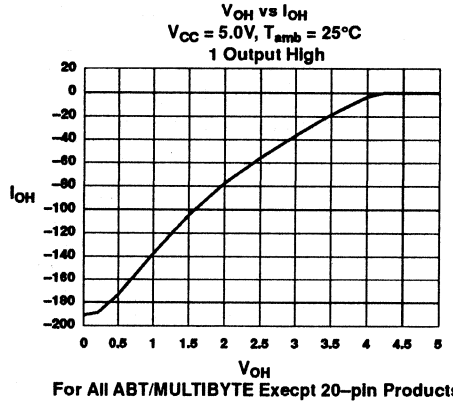
Introduction to ABT and MULTIBYTE



For All ABT/MULTIBYTE Products



For All ABT 20–pin Products



For All ABT/MULTIBYTE Execpt 20–pin Products

Figure 2. Voltage vs Current

OUTPUT CHARACTERISTICS

The BiCMOS interface devices have TTL output electrical levels, guaranteeing a V_{OL} of 0.55V (typically 0.4V) while sinking 64mA and guaranteeing a V_{OH} level of 2.0V (typically 3.1V) while sourcing 32mA. Unlike a pure bipolar output structure, these outputs will effectively "turn–off" when the output is in the High state or the disabled state and will not contribute to I_{CC}. This causes I_{CCH} and I_{CCZ} values to be essentially zero. When the output is in the Low state, the device will show some I_{CCL} but this value is less than most equivalent bipolar devices by a factor of three to four.

In order to effectively drive heavily loaded local bus applications or almost all backplane or system bus applications, high output current drivers are required. The Signetics ABT and MULTIBYTE devices provide as standard 64mA I_{OL}, enough current for nearly all bus driving applications. Figure 2 shows the output current versus voltage characteristic for an ABT output structure. This clearly shows the ability of the output to source and sink large amounts of current to and from the bus to which it is interfaced.

Introduction to ABT and MULTIBYTE

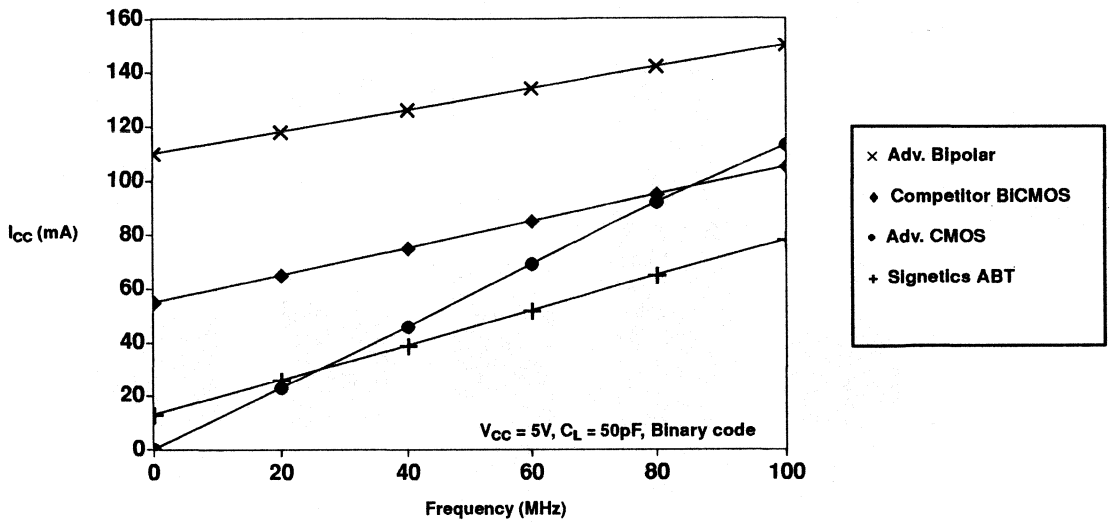


Figure 3. Current Consumption vs. Frequency (74ABT245 Function)

POWER DISSIPATION

Device power dissipation is of greater concern now than it was only a few years ago. The largest influence on this trend is almost certainly the move towards smaller, more compact systems and their related reliability concerns. Along with this, the increased popularity of surface mount devices has driven heat dissipation specifications towards zero. No longer can ten interface devices sitting disabled on a bus be allowed to dissipate five watts of power. The ABT and MULTIBYTE devices from Signetics will be guaranteed to dissipate typically zero power (mW) when disabled or in the High state.

It is certainly true that static power dissipation is not the entire story. The device, after all, will be in a critical path and will, therefore, be under some pressure from the devices to which they are interfaced to operate. Figure 3 illustrates the relative current consumption of a popular octal device when the device is under operation. Each output is loaded with a 50pF load and counts through a binary code from 00000000 to 11111111 at the given frequency.

It is common knowledge that pure CMOS devices perform rather poorly with respect to power dissipation at very high frequencies. It can also be noted, however, that pure bipolar devices also show a positive, non–zero slope of I_{CC} versus frequency. The figure shows that the ABT BiCMOS parts will consume roughly the same amount of delta current versus delta frequency (slope) as bipolar/other BiCMOS, but its overall magnitude is approximately 100mA less than a pure bipolar approach over the entire frequency range and 40mA less than a competing BiCMOS approach.

Introduction to ABT and MULTIBYTE

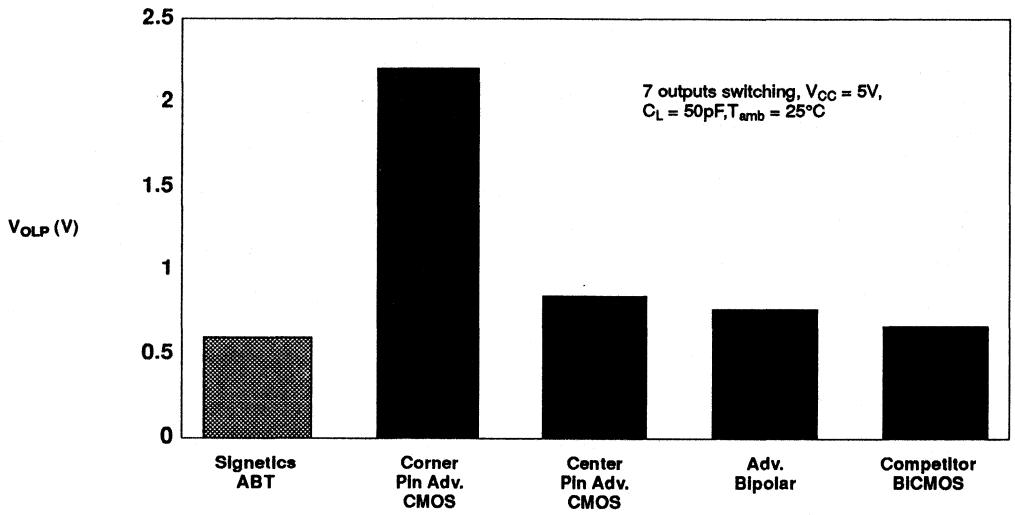


Figure 4. Ground Bounce Voltage (74ABT245 Function)

NOISE

Ground and V_{CC} noise generated by an integrated circuit has been greatly recognized as an undesirable feature that needs to be addressed by the IC manufacturer and not by the system designer alone. Supply noise causes numerous problems ranging from propagation delay degradation to logic errors to EMI/FCC failures. Considerable attention has been focused on noise and its related issues and Figure 4 shows a comparison of various devices available and their equivalent ground bounce voltage (V_{OLP}). Signetics 74ABTXXX devices have been responsibly designed to exhibit less than 800mV of ground noise which can be observed in Figure 4.

CONCLUSION

Signetics Advanced BiCMOS interface logic begins a new chapter in interface logic performance. Using a new revolutionary integrated bipolar and CMOS process, the devices allow for faster, high drive applications while lowering power dissipation to previously unreachable levels. High speed and high drive were not acquired at the cost of high power dissipation, increased bus loading, or increased noise. Together with support from the widest range international supplier of logic devices in the world, Signetics 74ABTXXX Advanced BiCMOS interface logic devices have become the high performance interface logic of choice.

Quality and Reliability

SIGNETICS' QUALITY PROGRAM

In 1979, Signetics recognized that quality was becoming a major competitive issue, not only in the semiconductor business but also in other industries. Increases in the volume of products imported from the Far East (steel, automobiles, and consumer products) sent strong signals that new competitive forces were at work.

An investigation into a variety of quality programs was started. The company realized that quality improvement would require a contribution from all employees. Management commitment and participation, however, was recognized as the primary prerequisite for this program to work successfully. Resources required for the resolution of defects were under management control.

In 1980 a program was developed which focused on quality management. Rearranging previous quality control philosophies, we developed a decentralized, distributed quality organization and simultaneously installed a Quality Improvement Process (QIP) based on the 14-Step improvement program advocated by Phil Crosby. The process was formally begun company-wide in 1981. Since then substantial progress has been made in every aspect of our operations. From incoming raw material conformance to improvements in clerical errors — every department and individual is involved and striving for Zero Defects. Zero Accept sampling plans and Zero Defects warranties are evidence of our ongoing commitment to and progress in quality. Over the past decade, Signetics has achieved a 90 fold improvement in product electrical quality, 30 fold improvement in product mechanical quality and a 20 fold improvement in product reliability.

Today the quality improvement process has evolved to Total Quality Management (TQM) having a far-reaching impact on all aspects of our business. Customers are provided with products of refined electrical and mechanical quality. TQM requires a clear set of management principles which mandate systems and measurements consistent with stated objectives. TQM endorses and utilizes the seven major examination categories of the U.S.A. Malcolm Baldrige National Quality Award. Together, the examination categories address all major components of an integrated, prevention based system built around continuous improvement and customer satisfaction.

ZERO DEFECTS WARRANTY

In recent years, American industry has demanded increased product quality of its IC suppliers in order to meet growing international competitive pressure. As a result of this quality focus, it is becoming clear that what once was thought to be unattainable— Zero Defects— is, in fact, achievable.

Signetics offers a Zero Defects Warranty which states that we will take back an entire lot if a single defective part is found. This precedent setting warranty implemented in 1985 effectively ended the IC industry's "war of the AQLs" (Acceptable Quality Levels). The ongoing efforts of IC suppliers to reduce PPM (Parts Per Million) defect levels is now a competitive customer service measure. This intense commitment to quality provides an advantage to today's electronics OEM. That advantage can be summed up in four words: ***Reduced Cost of Ownership.***

As IC customers look beyond purchase price to the total cost of doing business with a vendor, it is apparent that a quality-conscious supplier represents a viable cost reduction resource. Consistent high-quality circuits reduce requirements for expensive test equipment and personnel, and allow for smaller inventories, less rework, and fewer field failures. Programs such as Self Qualification and Ship-To-Stock implemented in 1984 and Cycle Time Management (CTM) implemented in 1990 help reduce cost of ownership.

STATISTICAL PROCESS CONTROL (SPC)

Although application of statistics in our process development and manufacturing activities goes back to the early 1970's, the corporate-wide emphasis on Statistical Process Control (SPC) did not come until mid-1984.

A natural evolution of our quality improvement process made introduction of SPC and other related programs an inevitable event. SPC was, therefore, introduced under the QIP umbrella. The Crosby definition of Quality, "Conformance To Requirements (Specification)" was expanded to include "Conformance To Specified Targets". The measurement definition of "continuous improvement" was expanded to include "Continuous Reduction of Variability Around the Specified Target".

The objective of SPC is to introduce a systematic and scientific approach to business and manufacturing activities. This approach utilizes sound statistical theory. Managers are expected to be able to turn data into information and to make decisions solely on data (not perception).

The most critical and challenging aspect of implementing SPC is the establishment of a discipline within the operating areas so that decision making is fundamentally based on verifiable data and so that actions are documented. The other is the realization that statistical tools merely point out the problems but are not themselves solutions. The burden of action on the process is still on the shoulders of the person that implemented it. In order to implement SPC effectively, three steps are continually followed:

Documenting and understanding the process and using process flow charts and component diagrams.

1. Establishing data collection systems and using SPC tools to identify process problems and opportunities for improvement.
2. Acting on the process and establishing guidelines to monitor and maintain process control.
3. Acting on the process and establishing guidelines to monitor and maintain process control.

Repeating steps 1-3 again.

These fundamentals are the basis of establishing specifications and operating philosophy with respect to SPC. We believe a solid foundation creates a permanent system and accelerates our quality improvement process.

CYCLE TIME MANAGEMENT

Cycle Time Management efforts are focused on Design-Development Process Responsiveness and Make-Market Process Responsiveness. Both are aimed at reducing the cycle time of tasks from current performance (Baseline) to entitlement (Using Existing Resources) then to improved entitlement and theoretical limit. Design-Development focuses on getting the right products and processes to production within the market window interval. Make-Market concentrates on getting product into the customers hands within Customer Lead Time Requirements. Cycle time management directly links to quality improvement in its requirement for task barrier identification at the root cause level and removal of those barriers (e.g. eliminating causes of rejects thereby eliminating rework or product sort). Also, the acceleration of results from reducing cycle time increases the frequency of events thereby increasing the cycles of learning required for quality improvement.

QUALITY PERFORMANCE

Our Quality Improvement Process has influenced our entire production cycle - from the purchases of raw materials to the shipment of finished product. The involvement of all areas of the company has resulted in

Quality and Reliability

impressive quality improvements. A traditional quality gauge is final electrical and visual/mechanical product defect levels as measured upon first submittal results at outgoing Quality Assurance gates; Estimated Process Quality. This is the PPM Level at our outgoing inspection for all accepted and rejected lots. (See Figures 1 and 2.) Current product shipments routinely record below 20PPM (Parts Per Million) electrical defect levels and 150PPM visual/mechanical defect levels. Since we utilize zero accept sampling on all finished production inspection, any lot with one or more rejects is 100 percent rejected.

The most meaningful measure in our product quality is how we measure up to our customer's expectations. Many customers routinely send us incoming inspection data on our products. One major mainframe manufacturer has reported zero defects in electrical, visual-mechanical, and hermeticity and has reported a 100 percent lot acceptance rate on the Standard Products Group product for over a year. Signetics is very appreciative of the recognition given by customers. In the past 3 years, Signetics has received over 50 formal commendation plaques from customers in recognition of Quality, Delivery and Service. Due to this type of performance, an increasing number of our customers are eliminating expensive incoming inspection testing and have begun implementation of the Ship-to-Stock Program. (See Figure 3.)

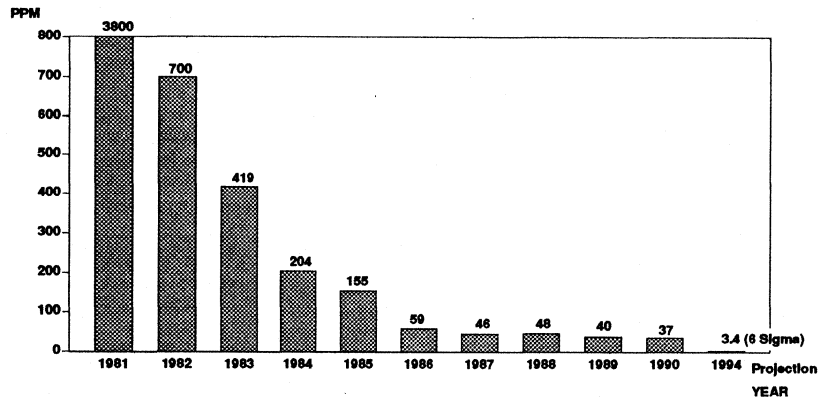


Figure 1. Electrical Product Quality Based on First Time Q.A. Submission Results

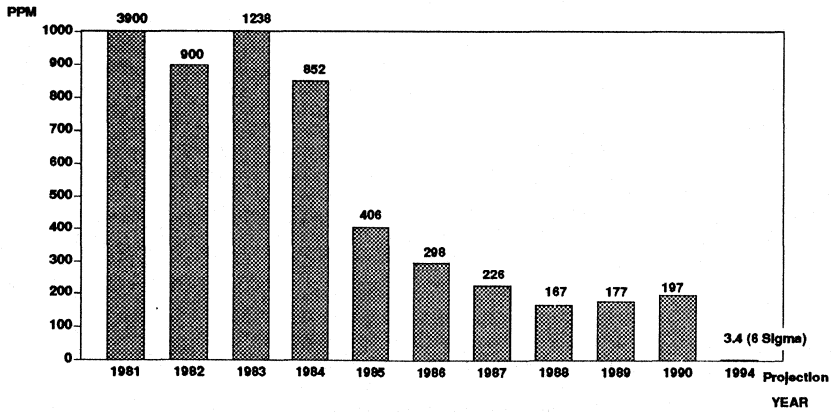
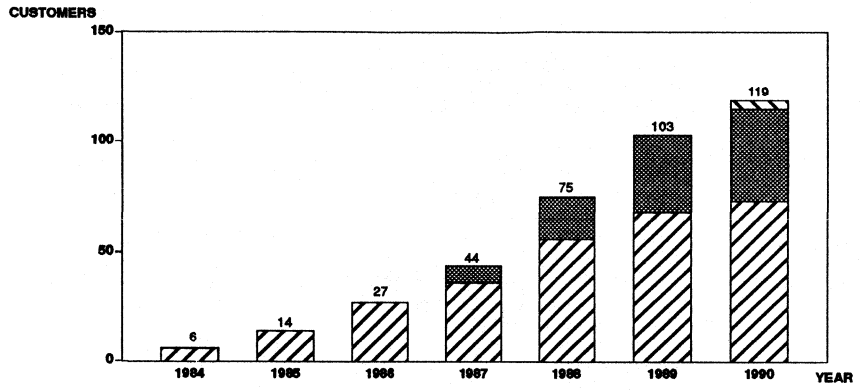


Figure 2. Visual/Mechanical Product Quality Based on First Time Q.A. Submission Results

Quality and Reliability



	1984	1985	1986	1987	1988	1989	1990
Asia Customers							4
Euro Customers				8	19	35	42
U.S. Customers	6	14	27	36	56	68	73

Figure 3. Signetics Ship-To-Stock Customer Growth

SHIP-TO-STOCK PROGRAM

Ship-to-Stock is a formal program developed at the request of our customers to help them reduce their costs by eliminating incoming test and inspection. Through close work with these customers in our quality improvement program, they became confident that our defect rates were so low that the redundancy of incoming inspections and testing was not only expensive, but unnecessary. They also saw that added component handling increased the potential of causing defects.

Ship-to-Stock is a joint program between Signetics and a customer which formally certifies specific parts to go directly into the customer's assembly line or inventory. This program was developed at the request of several major manufacturers after they had worked with us and had a chance to experience the data exchange and joint corrective action occurring as part of our quality improvement program.

Manufacturers using large volumes of ICs, those who are evaluating Just-in-Time delivery programs, or those who want to reduce or avoid high-cost incoming inspection are strongly encouraged to participate in this worthwhile program. Contact your local sales representative for further assistance and information on how to participate in this program.

SUMMARY

The Quality Improvement Program has had a far-reaching impact on all aspects of our business. It has, of course, provided our customers with products of improved electrical and mechanical quality and has provided us with a method of managing product reliability improvement to ensure that our products continue to perform as specified.

The corrective action teams that work to eliminate the cause of defects are committed to producing highly reliable integrated circuits and, as demonstrated by our continually improved product reliability performance, we are well on the way to achieving our objective, ZERO DEFECTS.

RELIABILITY ASSURANCE PROGRAMS

Focus on Product Reliability

From 1981 to 1984, continuing improvements in process and material quality had a significant impact on product reliability.

Since 1984, the company has intensified its effort to markedly improve product reliability. Corporate Reliability Engineering, Group and Plant Reliability Units and Manufacturing Engineering work jointly on numerous improvement activities. These focused activities enhance the reliability of future products by providing improved methods for reliability assessment, increased understanding of failure physics, advanced analytical techniques, and aid in the development of material and processes.

RELIABILITY MEASUREMENT PROGRAMS

Comprehensive product and process qualification programs have been developed to assure that our customers are receiving highly reliable products for their critical applications. Additionally, ongoing reliability monitoring programs, SURE III and Product Monitor, sample standard production on a regularly established basis (see Table 1).

Quality and Reliability

Table 1. Reliability Assurance Programs

RELIABILITY FUNCTION	TYPICAL STRESS	FREQUENCY
New Process Qualification	High Temperature Operating Life Temperature-Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle	Each new wafer fab process
New Product Qualification	High Temperature Operating Life Temperature-Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle Electrostatic Discharge Characterization	Each new product family
SURE III	High Temperature Operating Life Temperature-Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle	Each fab process family, every four weeks
Product Monitor	Pressure Pot	Each plastic package type and technology family at each assembly plant, every week

DESCRIPTION OF STRESSES

High Temperature Operating Life

Static High Temperature Life (SHTL) stressing applies static DC bias to the device. This has specific merit in detecting ionic contamination problems which require continuous uninterrupted bias to drive contaminants to the silicon surface. The voltage bias must be maintained until the devices are cooled down to room temperature from the elevated life test temperature. Dynamic High Temperature Life (DHTL) stressing is not as effective in detecting such problems because the bias continuously changes, intermittently generating and healing the problem. For this reason, SHTL has typically been used as the accelerated life stress for Logic products. DHTL is useful for products such as memory and micro-processor/controller where a large portion of the area can only be accessed by dynamic means.

HTSL-High Temperature Storage Life

This stress exposes the parts to elevated temperatures (150°C-175°C) with no applied bias. For plastic packages, 175°C is the high end of its safe temperature region without accelerating untypical failure mechanisms. This test is intended to accelerate potential mechanical package-related failure mechanisms such as Gold-Aluminum bond integrity and other process instabilities.

THBS-Temperature-Humidity, Biased, Static

The accelerated temperature and humidity bias is performed at 85°C and 85% relative humidity (85°C/ 85% RH). In general, the worst case bias condition is the one which minimizes the device power dissipations and maximizes the applied voltages. Higher power dissipations tend to lower the humidity level at the chip surface and lessen the corrosion susceptibility.

TMCL-Temperature-Cycling, Air to Air

The device is cycled between the specified upper and lower temperature without power in an air or Nitrogen environment. Normal temperature extremes are -65°C and +150°C with a minimum 10 minute dwell and 5 minute transition per MIL-STD-883C, Method 1010.5, Condition C. This is a good test to measure the overall package to die mechanical compatibility, because the thermal expansion coefficients of the plastic are normally very much higher than those of the die and leadframe. However, for large die the stress may be too severe and induce failures that would not be expected in a real application.

PPOT-Pressure Pot

This stress exposes the devices to saturated steam at elevated temperature and pressure. The standard condition is 20 PSIG which occurs at a temperature of 127°C and 100% RH. The stress is used to test the moisture resistance of plastic encapsulated devices. The plastic encapsulant is not a moisture barrier and will saturate with moisture within 72 hours. Since the chip is not powered up the chip temperature and relative humidity will be the same as the autoclave once equilibrium is reached. Because the steam environment has an unlimited supply of moisture and ample temperature to catalyze thermally activated events, it is effective at detecting corrosion problems, contamination induced leakage problems, and general glassivation stability and integrity. It is also a good test for both package integrity (cracks in the package), and for die cracks (the moisture swells the plastic enough to stress the die; also the moisture causes leakage paths in the crack itself).

PRODUCT AND PROCESS PROGRAMS

Qualification activity is centered around new products and processes and changes in products and processes. The goal is to assure that the products can meet the qualification requirements prior to general release, and on an ongoing basis to demonstrate conformance to those requirements. The nature and extent of reliability stressing required depends on the type of change and the amount of applicable reliability data available.

A full qualification may include Early Failure Rate (EFR), Intrinsic Failure Rate (IFR), and Environmental Endurance Stressing. Such stress plans are reserved for introductions or changes that involve new or untested material or processes and, as such should be subjected to the maximum reliability interrogation. This normally entails a full range of biased and unbiased temperature and humidity stresses along with thermo-mechanical stresses.

For changes that are of limited scope, the full range of qualification stressing may not be warranted. In these instances, the nature and extent of the change is examined and only those stresses which provide a valuable measure of the change, or those which will detect potential weakness, are performed.

Quality and Reliability

SELF-QUAL PROGRAM (SQP)

Self-Qual is a joint program between Signetics and a customer that formally communicates the qualification activities for a new or changed product, process, or material. The Self Qual process provides our customer's engineering groups an opportunity to participate in the development of the qualification plan. During the qualification process, customers may audit the project, and can receive interim updates of qualification progress. Upon completion, formal detailed engineering reports are provided.

The major impact to the customer comes from the reduced workload on the component engineering and qualification groups. These engineering resources generally divide their time between routine qualification activity and problem resolution on critical components. By eliminating the need to perform qualification for one of the basic vendor changes the customer component engineer can spend more of his time resolving the critical product issues. In addition, the total amount of stress hardware needed to perform qualification life tests and other environmental evaluations can be reduced, saving the customer facility costs and reducing operating expense.

Self-Qual is a no-risk proposition for the customer. Each Self-Qual proposal provides a detailed description of what we are changing and why. It includes a detailed plan of what we intend to do to establish the reliability of the products affected. If the customer wishes to have product added to the plan or select some additional stresses, or prefers alternative stress conditions, Signetics will do everything possible to accommodate those requests. After that, if the customer is still uncomfortable with the recommended change, they are under no obligation to accept our data, and they may also perform their own qualification program. Customers who are interested in participating in this program should contact their local sales representative or the Corporate Reliability Engineering department directly.

SURE III RELIABILITY MONITORING PROGRAM

In order to implement an improvement program, a standard measure of performance was needed. The results from the SURE III Reliability Monitoring Program are used as basic ongoing measures of product reliability performance. This program samples all generic families of products manufactured and utilizes standardized stress methods and test procedures. This system is augmented by new product and process qualification activities and infant mortality monitoring programs. A measurement philosophy was adopted based on the premise of continual improvement toward our performance standard of zero defects. We also increased our standard Pressure Pot stress conditions from 15 PSIG/1215C to 20 PSIG/1275C. This reduced stress duration from 168 hours to 72 hours, and increased high volume sampling, which increased sensitivity to low defect levels. Our standard monitoring program, SURE III, includes the stress conditions as described in Table 2. The continuous improvement results are shown in Figure 4. Signetics Reliability Index as Failure Per Million (FPM). The FPM value includes all rejects from all accelerated stresses divided by total units submitted to all stresses. This is a relative number used to manage continuous reliability improvement. It should not be interpreted as an expected failure rate. Failure rate information is provided in the Signetics Product Reliability Summary Report available to all customers.

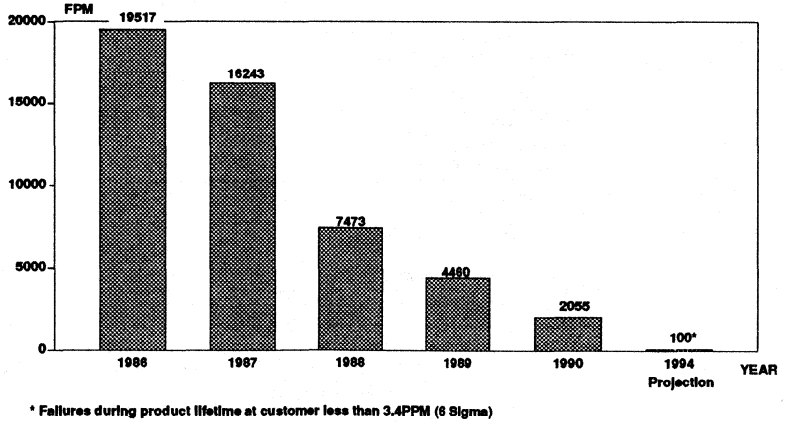


Figure 4. Signetics Reliability Index

Quality and Reliability

PRODUCT MONITOR

In addition to the SURE III program, each assembly plant performs Pressure Pot (20PSIG, 1275C, 72hours) reliability monitors on a weekly basis for each molded package type by pin count. The purpose of this program is to monitor the consistency of the assembly operations for such attributes as molding quality and die attach and wire bond integrity. This data is reported back to manufacturing operations and corporate and group reliability and quality assurance departments by electronic mail each week.

RELIABILITY EVALUATION

In addition to the product performance monitors encompassed in the SURE III program, Corporate and Group Reliability Engineering departments sustain a broad range of evaluation and qualification activities. Included in the engineering process are:

- Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities, and subcontractors.
- Devices or generic group failure rate studies.
- Advanced environmental stress development.
- Failure mechanism characterization and corrective action/prevention reporting.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE III program; however, more highly accelerated conditions and extended durations typify these engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are often included in some evaluation programs.

STRESS FACILITY QUALITY

Quality improvement has reached all functional areas of the company, and the reliability stress laboratories are no exception. Corporate Reliability Laboratory (CRL) is one of the many areas where the benefits of the quality improvement process pays repeated dividends.

CRL utilizes stress which accelerate failure rates hundreds to thousands of times, requiring precision and control to make reliability data meaningful. Stress loading schedules are maintained with absolute regularity and chambers are never off-line beyond scheduled loading plans. Board currents are recorded prior to and at each interval on biased stresses, and monitoring of in-oven currents is conducted daily.

Thermal modeling of the Temperature Cycling systems has been accomplished and all loads are carefully weighed to ensure that thermal ramps are consistent.

Pressure Pot and Biased Pressure Pot systems utilize microprocessor controllers, and are accurate to within 0.1 degree centigrade. Saturation is guaranteed via automatic timing circuits, and a host of fail-safe controls ensure that test groups are never damaged.

Electrostatic discharge (ESD) handling precautions are standard procedures in the laboratories, and the occurrences of devices lost, zapped, or overstressed have become almost non-existent.

Table 2. SURE III Reliability Monitoring Programs

RELIABILITY FUNCTION	STRESS CONDITIONS
Static High Temperature Operating Life (SHTL)	$T_J \geq 150°C$, $T_A = 125°C$ to $150°C$, Biased condition = Static, V_{CC} = MAX, Duration = 1000 hours
High Temperature Storage Life (HTSL)	$T_A = 150°C$, Biased condition = None, Duration = 1000 hours
Temperature-Humidity, Biased, Static (THBS)	$T_A = 85°C \pm 3°C$, Humidity = 85% RH ± 5%, Biased condition = Static, V_{CC} = MAX, Duration = 1000 hours
Temperature Cycling (TMCL)	T_A = -65°C (+0°C -10°C) to +150°C (+10°C -0°C), Air-to-Air, Dwell time = 10 minutes minimum each extreme, Biased condition = None, Duration = 1000 cycles for plastic package, 300 cycles for ceramic package
Pressure Pot	$T_A = 127°C \pm 2°C$, 20 PSIG ±0.5 PSIG (PPOT). 100% saturated steam, Biased condition = None, Duration = 72 hours

NOTE: V_{CC} = MAX is generally equal to V_{CC} = MAX as specified in data handbook

Quality and Reliability

RELIABILITY IMPROVEMENT PROGRAMS

Recent reliability improvement programs that enhance product reliability performance include a series of activities addressing failure rate reduction in thermal cycling stresses, particularly on large die. Other reliability improvement programs involved the use of Silicon Nitride and other technologically advanced passivation systems to increase the high humidity resistance of sensitive products.

Reducing early life failures became a major focus in 1986. Numerous corrective action teams established high volume monitors capable of accurately describing parts per million (PPM) level infant failure rates. From data produced via these monitors, improvement in wafer fabrication process and assembly process technologies occurred to minimize integrated circuits defect levels. The Early Failure Rate (EFR) level was driven from 521 FPM in 1987, 398 FPM in 1988, 252 FPM in 1989 to less than 100 FPM in 1990.

MANUFACTURING FACILITIES

Signetics, as part of a multinational corporation, utilize manufacturing facilities for wafer fabrication, package assembly, and test in three states and five overseas countries as shown in Table 3. Wafer fabrication is performed in fabs which report to the Product Groups. Assembly operations in Utah, Korea, and Thailand report to the Vice President of Assembly Manufacturing Operations (AMO). Assembly subcontractors (Alphatec, Anam, Hyundai, MEC, Pebei, Team and Rohm) are scheduled and controlled through the AMO organization. Assembly subcontractors process all product to Signetics' specifications and materials. We have on-site quality assurance personnel at each subcontractor site to audit assembly processes and procedures.

TYPICAL IC MANUFACTURING FLOW

The manufacturing process for integrated circuits begins with wafer fabrication. The wafers are then electrically sorted, assembled, and tested prior to customer shipment. Quality assurance inspections are utilized throughout the manufacturing process.

Table 3. Product Manufacturing

FACILITIES	DESIGNATION	LOCATION	PROCESS OR PACKAGE FAMILIES
Wafer Fabrication	Fab 01	Sunnyvale, California, USA	Bipolar, Linear, Junction Isolated and Quality Assurance
	Fab 21	Orem, Utah, USA	Bipolar Gold Doped, Schottky, Oxide Isolated, ECL, PLD and Quality Assurance
	Fab 22	Albuquerque, New Mexico, USA	NMOS, CMOS, ACMOS, BiCMOS, EPROM and Quality Assurance
	Fab 23	Albuquerque, New Mexico, USA	CMOS EPROM, Flash EPROM and Quality Assurance
	Fab 92 (MOS #2)	Nijmegen, The Netherlands	HC(T) CMOS Logic and Quality Assurance
Assembly	Alphatec	Bangkok, Thailand	Ceramic DIP and Quality Assurance
	Anam	Seoul, Korea	Plastic SO, PLCC, Metal Can and Quality Assurance
	Hyundai	Ichon, Kyungki, Korea	Plastic DIP, Ceramic DIP and Quality Assurance
	MEC	Osaka, Japan	Plastic SO EIAJ, QFP and Quality Assurance
	Orem	Orem, Utah, USA	Ceramic DIP, Flat Pack, QFP, PGA and Quality Assurance
	Pebei	Kaosiung, Taiwan	Plastic DIP, SO, SSOP, PLCC, and Quality Assurance
	SigKor	Seoul, Korea	Plastic DIP, SO, PLCC, and Quality Assurance
	Sig Thai	Bangkok, Thailand	Plastic DIP and Quality Assurance
	Team	Manila, Philippines	Plastic DIP and Quality Assurance
	Rohm	Kyoto, Japan	Plastic QFP and Quality Assurance
Test	TA03/04	Sunnyvale, California, USA	Wafer Sort, Final Test and Quality Assurance
	SigKor	Seoul, Korea	Final Test and Quality Assurance
	SigThai	Bangkok, Thailand	Final Test and Quality Assurance
	Albuquerque	Albuquerque, New Mexico, USA	Wafer Test and Quality Assurance
	Orem	Orem, Utah, USA	Military Final Test and Quality Assurance

Quality and Reliability

Table 4. Package Construction

ITEMS	PLASTIC DIP	SO AND PLCC	CERAMIC DIP(CERDIP)	CERAMIC FLAT PACK
Lead Frame	Copper, 194 Alloy	Copper, 194 or PMC102	Alloy-42	Alloy-42
Lead Finish	Tin/Lead Solder Dip (60/40)	Tin/Lead Solder Dip (60/40) or Solder Plate (80/20)	Tin/Lead Solder Dip (60/40)	Tin/Lead Solder Dip (60/40)
Bond Area Finish	Silver Spot	Silver Spot	Silver Spot	Silver Spot
Die Attach	Silver Filled Polymide or Thermoplastic	Silver Filled Polymide or Thermoplastic	Silver Filled Glass	Silver Filled Glass
Bond Wire	Gold, 1.0-1.3 mils in Diameter	Gold, 1.0-1.3 mils in Diameter	Aluminum, 1.0-1.3 mils in Diameter	Aluminum, 1.0-1.3 mils in Diameter
Wire Bonding Die Lead Frame	Thermosonic Ball Stitch	Thermosonic Ball Stitch	Ultrasonic Stitch Stitch	Ultrasonic Stitch Stitch
Package Material	Novolac Epoxy	Novolac Epoxy	Ceramic	Ceramic

SPECIAL PROCESSING

SUPR II LEVEL B –

For our customers who require an infant mortality rate level less than that normally provided for our standard products (typically less than 1000PPM), we offer our Signetics Upgraded Product Reliability (SUPR) program.

Devices are burned-in per Signetics specification 850-227 schematics for a minimum of 21 hours at junction temperature between 155°C to 175°C. For a 1.0eV activation energy, 21 hours at 155°C is equivalent to 168 hours at 125°C.

Following burn-in, all devices are cooled down under bias and tested within 96 hours. All devices are tested before and after burn-in, yield calculated and compared to Percent Defective Allowed (PDA). If a lot fails PDA, it is investigated and good units submitted to a second burn-in. All "SUPR II B" devices carry a "B" marking.

The SUPR program was introduced in 1972 to improve quality and reliability and was expanded in 1975 to SUPR II A which included the burn-in option, SUPR II B. With the implementation of the Signetics Quality Improvement Process in 1980, standard product quality levels and guarantees caught up and passed SUPR II. All processing, except for burn-in, is now standard. The Signetics standard warranty is Zero Defects.

"Evaluation of Early Failure Levels and The Effectiveness of Burn-In" is available upon request through your local sales office. This brochure is an aid for those users and purchasers of integrated circuits who need to make a decision regarding burn-in.

PUBLICATIONS

Signetics routinely publishes documents supporting the Quality and Reliability Improvement Process. The following significant documents are currently available.

IC Quality Series

Quality and Reliability Policy Manual (850-8000)

This manual is the starting point for understanding the policies of Signetics pursuant to constantly improving the high standards of quality and reliability in the manufacture of monolithic integrated circuits. Responsibilities and authority of organizations are defined along with governing specifications and operator instruction documents.

Supplier Partnership Guide

This booklet defines Signetics philosophy, policy and requirements for establishing strategic partnerships with raw material suppliers.

Product Symbol Formats

This publication provides a guide for determining standard product symbol format and content for decoding inventory and product in field usage since 1980. Since date code 8717, Signetics has symbolized the assembly start computer Lot ID on commercial products providing full traceability back to start of wafer fabrication.

Quality Attributes EDI System

This manual defines system requirements for Electronic Data Interchange (EDI) of Quality Attributes (pass/fail) Data.

Monthly Product Outgoing Quality Summary Reports

Estimated Process Quality (EPQ) in PPM for electrical, visual/ mechanical and hermetical by part number or by family.

Statistical Process Control

This booklet introduces the Signetics SPC system including terminologies, philosophy, organization, training and implementation strategy and status.

Ship-To-Stock Program

This booklet defines the "joint program" requirements of Signetics and the customer to formally certify specific products to go directly into the assembly line or inventory with reduced or no incoming inspection thereby reducing cost of ownership.

Customer Return Immediate Service Program (CRISP)

This booklet defines the joint responsibilities of Signetics and the customer to assure that correlation samples are investigated and results reported per the Signetics 1-4-5 cycle time commitments.

Quality and Reliability Improvement Process

This booklet tells the story of the 1980 Signetics Quality Improvement Program evolving into the Quality Improvement Process (QIP) which is the foundation of all Signetics efforts aimed at total customer satisfaction. The March 1988 publication describes the story. More recent booklets contain updated foils only, without much text.

Quality and Reliability

IC Reliability Series

Signetics Reliability Handbook

This handbook is a detailed guide to Signetics Reliability Qualification and Monitoring activities. It includes reference sections that deal with the application and statistics of integrated circuit reliability issues.

Product Reliability Summary

Yearly, SURE III monitoring data is summarized and published for all product families in a Product Reliability Summary. Summaries like this one provide a detailed overview of product family performance and estimates the reliability of those products in use conditions.

Quarterly Reliability Update

Detailed results, by part number, package type, date code, assembly location, and by stress and test interval are routinely published in the Signetics Quarterly Reliability Update. The "Update" is available at the end of each quarter, and contains the results of reliability monitors which completed during the previous quarter, plus approximately 3 years of history for each product family.

SMD Reliability (The Reliability and Durability of Surface Mount Packages)

In support of Signetics' leadership in Surface Mount Device (SMD) technology, we have published in-depth studies and evaluations on the reliability and durability of SMD packages. The Surface Mount Reliability report covers evaluation of products after exposure to the unique environments created by various SMD soldering and cleaning processes.

Process Technology and Manufacturing Facility Roadmap

This document defines the various process technologies in production in Signetics manufacturing facilities, and defines in detail, the fab and assembly processes and locations qualified to produce all released products.

Thermal Characteristics of Integrated Circuit Packages

This is a comprehensive collection of thermal characterization data for all packages manufactured by Signetics. Thermal resistance data to *Case*, and to *Ambient* are provided. Details on airflow effects and die size are included.

SSQP – Signetics Self-Qual Program-Reports

In addition to the regular publications of reliability monitor results, a special program for the publication of qualification proposals and final engineering reports has been in place since January of 1984. Self-Qual Reports are available on all major process changes and introductions, thereby reducing customer cost of ownership.

Evaluation of Early Failure Levels and the Effectiveness of Burn-In

This report provides results of the Signetics Early Failure Rate (EFR) program implemented in 1986 to identify and eliminate root causes of infant mortality and to aid users of IC components faced with a decision regarding Burn-In of purchased integrated circuits.

DATA AVAILABILITY

The previously referenced documents are available to all our customers. Many are available in your local sales office, or from:

Corporate Quality System Group
Mail Stop #35
811 East Arques Avenue
P. O. Box 3409
Sunnyvale, CA 94088-3409, USA

where you can be placed on a standard mailing list for all documentation which meet your requirement(s).

Section 3
Family Specifications

INDEX

Family Specifications

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire 74ABT family, unless otherwise specified in the individual device data sheet.

INTRODUCTION

The 74ABT Advanced BiCMOS family combines the low power dissipation and low noise of BiCMOS with the high speed and high output drive of our bipolar modules.

The basic family of devices designated as 74ABTXXX will operate at BiCMOS input logic levels for high noise immunity, negligible quiescent supply and input current. It is operated from a power supply of 4.5 to 5.5V.

HANDLING MOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

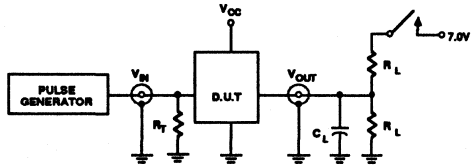
Family Specifications

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

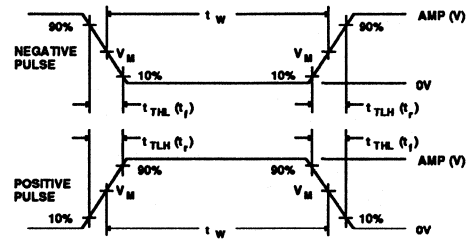
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

Data Sheet Specification Guide

INTRODUCTION

The 74ABT data sheets have been designed for ease-of-use. A minimum of cross-referencing for more information is needed.

TYPICAL PROPAGATION DELAY AND FREQUENCY

The typical propagation delays listed at the top of the data sheets are the average of t_{PLH} and t_{PHL} for a typical data path through the device with a 50pF load.

For clocked devices, the maximum frequency of operation is also given. The typical operating frequency is the maximum device operating frequency with a 50% duty factor and no constraints on t_R and t_F.

LOGIC SYMBOLS

Two logic symbols are given for each device - the conventional one (Logic Symbol) which explicitly shows the internal logic (except for complex logic) and the IEEE/IEC Logic Symbol.

The IEEE/IEC has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic current to each output without explicitly showing the internal logic.

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings table lists the maximum limits to which the device can be subjected without damage. This does not imply that the device will function at these extreme conditions, only that, when these conditions are removed and the device operated within the Recommended Operating Conditions, it will still be functional and its useful life will not have been shortened.

RECOMMENDED OPERATING CONDITIONS

The "Recommended Operating Conditions" table lists the operating ambient temperature and the conditions under which the limits in the "DC Characteristics" and "AC Characteristics" table will be met. The table should not be seen as a set of limits guaranteed by the manufacturer, but as the conditions used to test the devices and guarantee that they will then meet the limits in the DC and AC Characteristics tables.

TEST CIRCUITS

Good high-frequency wiring practices should be used in test circuits. Capacitor leads should be as short as possible to minimize ripples on the output waveform transitions and undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{CC} decoupling capacitor should be provided at the test socket, also with short leads. Input signals should have rise and fall times of 2.5ns, a signal swing of 0V to 3.0V; a 5MHz square wave is recommended for most propagation delay tests. The repetition rate must be increased for testing f_{MAX}. Two pulse generators are usually required for testing such parameters as setup time, hold time and removal time. f_{MAX} is also tested with 2.5ns input rise and fall times, with a 50% duty factor, but for typical f_{MAX} as high as 150MHz, there are no constraints on rise and fall times.

DC CHARACTERISTICS

The "DC Characteristics" table reflects the DC limits used during testing. The values published are guaranteed.

The threshold values of V_{IH} and V_{IL} are applied to the inputs, the output voltages will be those published in the "DC Characteristics" table. There is a tendency, by some, to use the published V_{IH} and V_{IL} thresholds to test a device for functionality in a "function-table exerciser" mode. This frequently causes problems because of the noise present at the test head of automated test equipment with cables up to 1 meter. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, in the order of milliseconds, so that there is no noise at the inputs when the outputs are measured. But in functionality testing, the outputs are measured much faster, so there can be noise on the inputs, before the device has assumed its final and correct output state. Thus, never use V_{IH} and V_{IL} to test the functionality of any ABT device type; instead, use input voltages of V_{CC} (for the High state) and 0V (for the Low state). In no way does this imply that the devices are noise-sensitive in the final system.

In the data sheets, it may appear strange that the typical V_{IL} is higher than the maximum V_{IL}. However, this is because V_{ILMAX} is the maximum V_{IL} (guaranteed) for all devices that will be recognized as a logic Low. However, typically a higher V_{IL} will also be recognized as a logic Low. Conversely, the typical V_{IH} is lower than its minimum guaranteed level.

AC CHARACTERISTICS

The "AC Characteristics" table lists the guaranteed limits when a device is tested under the conditions given in the AC Test Circuits and Waveform section.

Propagation delay

The data included in this section is meant to aid the designer in understanding system performance over a wider range of operating temperatures and load conditions, as well as at varying voltages. It should be noted that these design characteristics are not 100% tested but should very closely reflect actual device performance over the ranges specified.

Definitions of Symbols

DEFINITIONS OF SYMBOLS AND TERMS USED IN ABT DATA SHEETS

Current

Positive current is defined as conventional current flow into a device.

Negative current is defined as conventional current flow out of a device.

I_{CCH} Quiescent power supply current; the current flowing into the V_{CC} supply terminal when the output is at the High level.

I_{CCL} Quiescent power supply current; the current flowing into the V_{CC} supply terminal when the output is at the Low level.

I_{CCZ} Quiescent power supply current; the current flowing into the V_{CC} supply terminal when the output is in the disabled mode.

ΔI_{CC} Additional quiescent supply current per input pin at a specified input voltage and V_{CC}.

I_{GND} Quiescent power supply current; the current flowing into the GND terminal.

I_I Input leakage current; the current flowing into a device at a specified input voltage and V_{CC}.

I_{IK} Input diode current; the current flowing into a device at a specified input voltage.

I_{IO} Input/output source or sink current; the current flowing into a device at a specified input/output voltage.

I_O Output source or sink current; the current flowing into a device at a specified output voltage.

I_{OH} High level output source current; the current into an output with input conditions applied that, according to the product specification, will establish a High level at the output. Current out of the output is given as a negative value.

I_{OL} Low level output source current; the current into an output with input conditions applied that, according to the product specification, will establish a Low level at the output. Current out of the output is given as a negative value.

I_{OK} Output diode current; the current flowing into a device at a specified output voltage.

I_{OZ} OFF-state output current; the leakage current flowing into the output of a 3-State device in the OFF-state, when the output is connected to V_{CC} or GND.

Voltages

All voltages are referenced to GND (ground), which is typically 0V.

GND Supply voltage; for a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages; typically ground.

V_{CC} Supply voltage; the most positive potential on the device.

V_{EE} Supply voltage; one of two (GND and V_{EE}) negative power supplies.

V_H Hysteresis voltage; difference between the trigger levels when applying a positive and a negative-going input signal.

V_{IH} High-level input voltage; the range of input voltages that represents a logic High-level in the system.

V_{IL} Low-level input voltage; the range of input voltages that represents a logic Low-level in the system.

V_{OH} High-level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a High-level at the output.

V_{OHP} Maximum (peak) voltage induced on a quiescent High-level output during switching of other outputs.

V_{OHV} Minimum (valley) voltage induced on a quiescent High-level output during switching of other outputs.

V_{OL} Low-level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a Low-level at the output.

V_{OLP} Maximum (peak) voltage induced on a quiescent Low-level output during switching of other outputs.

V_{OLV} Minimum (valley) voltage induced on a quiescent Low-level output during switching of other outputs.

V_{T+} Trigger threshold voltage; positive-going signal.

V_{T-} Trigger threshold voltage; negative-going signal.

Definitions of Symbols

Capacitances

C_I Input capacitance; the capacitance measured at a terminal connected to an input of a device.

$C_{I/O}$ Input/Output capacitance; the capacitance measured at a terminal connected to an I/O pin (e.g. a transceiver).

C_L Output load capacitance; the capacitance connected to an output terminal including jig and probe capacitance.

C_{PD} Power dissipation capacitance; the capacitance used to determine the dynamic power dissipation per logic function when no extra load is provided to the device.

AC Switching Parameters

f_I Input frequency; for combinatorial logic devices the maximum number of inputs and outputs switching in accordance with the device function table. For sequential logic devices the clock frequency using alternate High and Low for data input or using the toggle mode, whichever is applicable.

f_O Output frequency; each output.

f_{MAX} Maximum clock frequency; clock input waveforms should have a 50% duty factor and be such as to cause the outputs to be switching from 10% V_{CC} to 90% V_{CC} in accordance with device function table.

t_H Hold time; the interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.

t_R, t_F Clock input rise and fall times; 10% and 90% values.

t_{PHL} Propagation delay time: The time between specified reference points on the input and the output waveforms with the output changing from the defined High-level to Low-level.

t_{PLH} Propagation delay time: The time between specified reference points on the input and the output waveforms with the output changing from the defined Low-level to High-level.

t_{PHZ} Output Disable time from High level to a 3-State output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from the High-level to a high impedance "OFF" state.

t_{PLZ} Output Disable time from Low level of a 3-State output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from the Low-level to a high impedance "OFF" state.

t_{PZH} Output Enable time to a High level of a 3-State output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from a high impedance "OFF" state to a High-level.

t_{PZL} Output Enable time to a Low level of a 3-State output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from a high impedance "OFF" state to a Low level.

t_{REC} Recovering time: The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.

t_S Setup time; the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval data to be recognized must be maintained at the input to ensure their recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{THL} Output transition time; the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from High-to-Low.

t_{TLH} Output transition time; the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from Low-to-High.

t_W Pulse width: The time between the reference point on the leading and trailing edges of a pulse.

Section 4
ABT Bus Interface Logic Data Sheets

INDEX

Quad buffer (3-State) — 74ABT125

FEATURES

- Quad bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT125 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT125 device is an quad buffer that is ideal for driving bus lines. The device features four Output Enables ($\overline{OE}0$, $\overline{OE}1$, $\overline{OE}2$, $\overline{OE}3$), each controlling one of the 3-State outputs.

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}n$	Dn	Qn
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

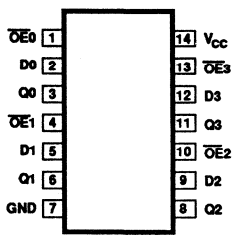
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP	-40°C to +85°C	74ABT125N
14-pin plastic SOL	-40°C to +85°C	74ABT125D

PIN DESCRIPTION

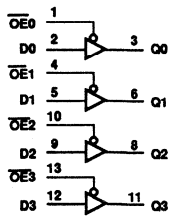
PIN NUMBER	SYMBOL	FUNCTION
2, 5, 9, 12	D0 - D3	Data inputs
3, 6, 8, 11	Q0 - Q3	Data outputs
1, 4, 10, 13	$\overline{OE}0$ - $\overline{OE}3$	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

PIN CONFIGURATION

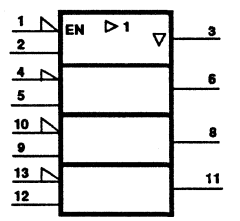


Top view

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Quad buffer (3-State) 74ABT126

FEATURES

- Quad bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT126 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT126 device is an quad buffer that is ideal for driving bus lines. The device features four Output Enables (OE0, OE1, OE2, OE3), each controlling one of the 3-State outputs.

FUNCTION TABLE

INPUTS		OUTPUT
OEn	Dn	Qn
H	L	L
H	H	H
L	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

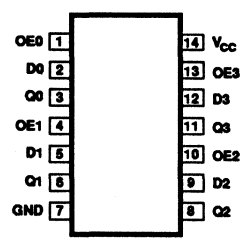
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP	-40°C to +85°C	74ABT126N
14-pin plastic SOL	-40°C to +85°C	74ABT126D

PIN DESCRIPTION

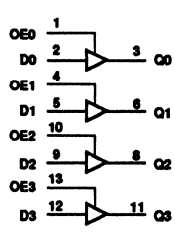
PIN NUMBER	SYMBOL	FUNCTION
2, 5, 9, 12	D0 - D3	Data inputs
3, 6, 8, 11	Q0 - Q3	Data outputs
1, 4, 10, 13	OE0 - OE3	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

PIN CONFIGURATION

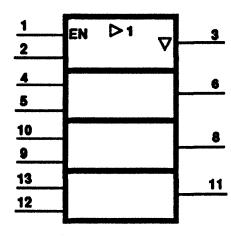


Top view

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Octal inverting buffer (3–State) 74ABT240

FEATURES

- Octal bus interface
- 3–State buffers
- Output capability: +64mA/–32mA
- Latch–up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT240 high–performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT240 device is an octal inverting buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3–State outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	C_L = 50pF; V_{CC} = 5V	3.5	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Ouputs disabled; V_{CC} =5.5V	500	nA

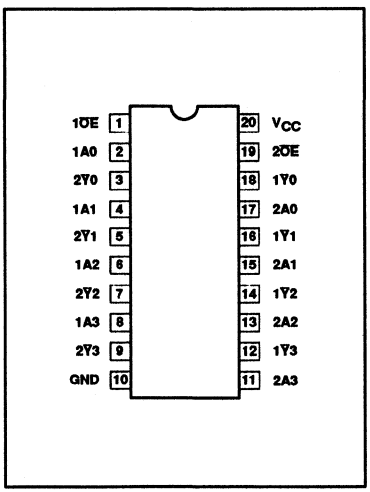
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20–pin plastic DIP	–40°C to +85°C	74ABT240N
20–pin plastic SOL	–40°C to +85°C	74ABT240D

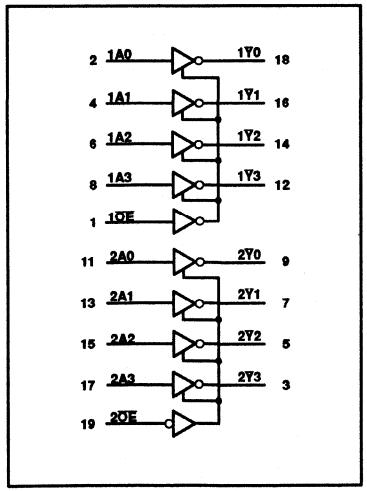
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11, 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	$1\overline{Y}0$ – $1\overline{Y}3$	Data outputs
9, 7, 5, 3	$2\overline{Y}0$ – $2\overline{Y}3$	Data outputs
1, 19	$1\overline{OE}$, $2\overline{OE}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

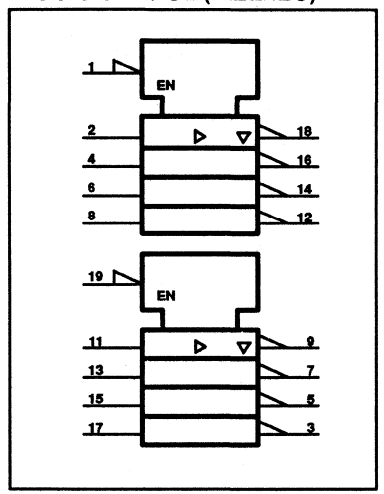
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS				OUTPUTS	
$1\overline{OE}$	1An	$2\overline{OE}$	2An	$1\overline{Y}n$	$1\overline{Y}n$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1 Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
2. The performance capability of a high–performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3 The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		–32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	operating free–air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High–level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low–level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3–State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3–State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_O	Short–circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		0.5	mA
		Outputs 3–State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3–State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		0.5	mA

NOTES:
1 Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2 This is the increase in supply current for each input at 3.4V.

Octal buffer/line driver (3-State) — 74ABT241

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT241 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT241 device is an octal buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, 2OE), each controlling four of the 3-State outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT241N
20-pin plastic SOL	-40°C to +85°C	74ABT241D

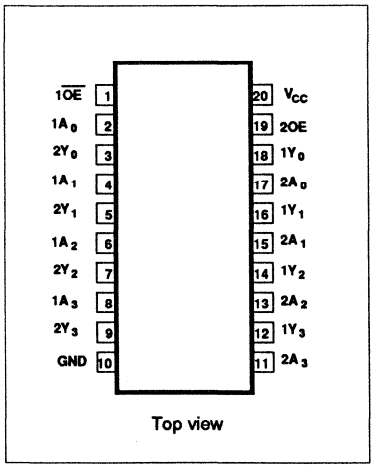
FUNCTION TABLE

INPUTS				OUTPUT	
$1\overline{OE}$	1An	2OE	2An	1Yn	2Yn
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

PIN DESCRIPTION

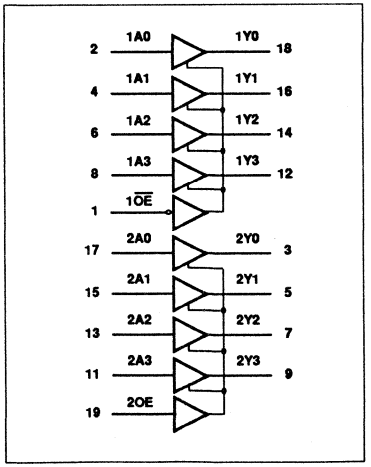
PIN NUMBER	SYMBOL	FUNCTION
2, 4, 6, 8	1A0 - 1A3	Data inputs
17, 15, 13, 11	2A0 - 2A3	Data inputs
18, 16, 14, 12	1Y0 - 1Y3	Data outputs
3, 5, 7, 9	2Y0 - 2Y3	Data outputs
1, 19	$1\overline{OE}$, 2OE	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

PIN CONFIGURATION

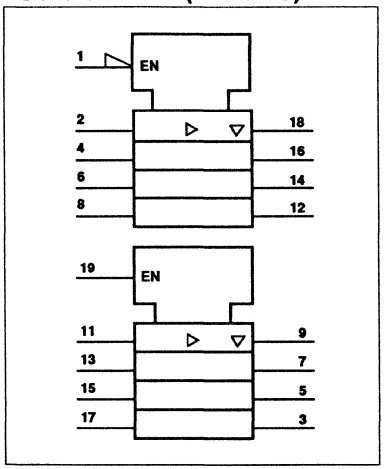


Top view

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

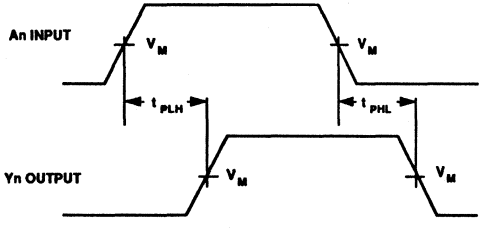
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

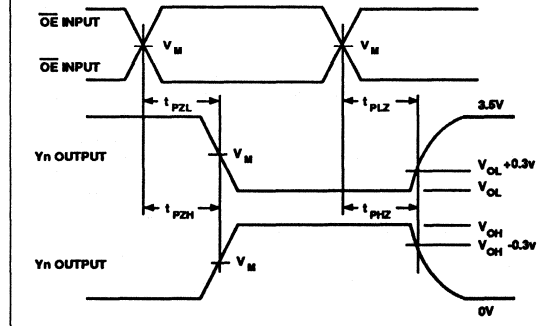
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Yn	1	1.0 1.0	2.6 2.9	4.1 4.2	1.0 1.0	4.6 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 1.3	3.0 4.3	6.3 5.8	1.1 1.3	6.8 6.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.6 1.0	4.6 3.9	6.1 5.4	1.6 1.0	7.1 5.9	ns

AC WAVEFORMS

(V_M = 1.5V, V_{IN} = GND to 3.0V)

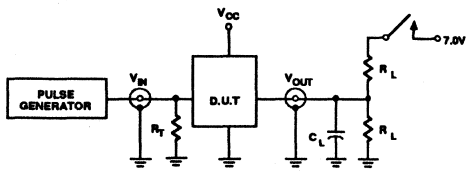


Waveform 1. Waveforms Showing the Input (An) to Output (Yn) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

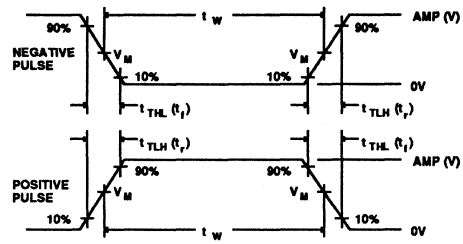
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

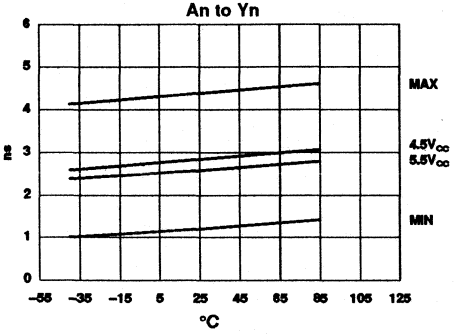


V_M = 1.5V

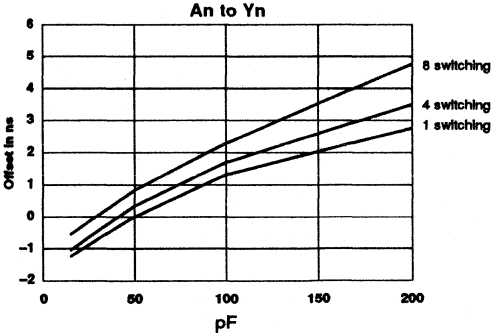
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

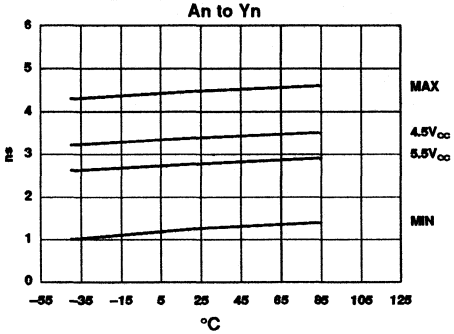
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
An to Yn



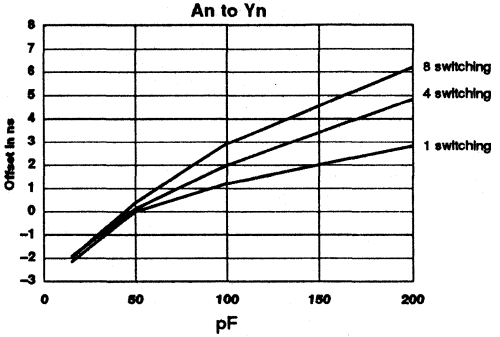
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
An to Yn



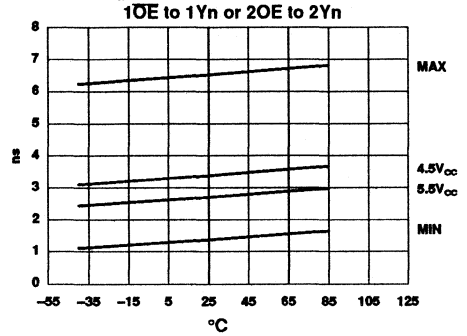
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
An to Yn



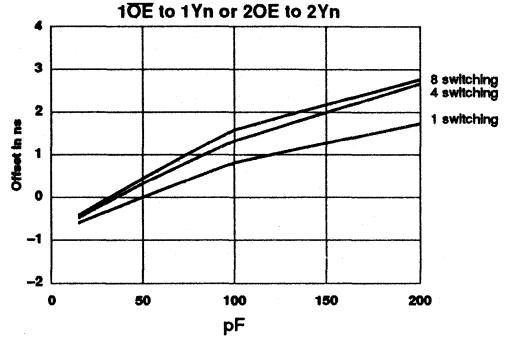
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
An to Yn



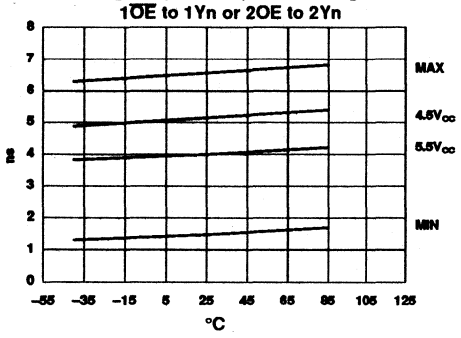
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$1\overline{OE}$ to 1Yn or $2\overline{OE}$ to 2Yn



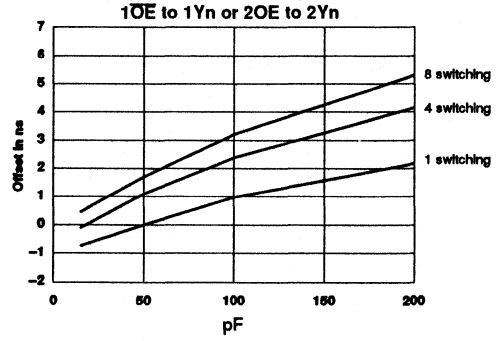
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$1\overline{OE}$ to 1Yn or $2\overline{OE}$ to 2Yn



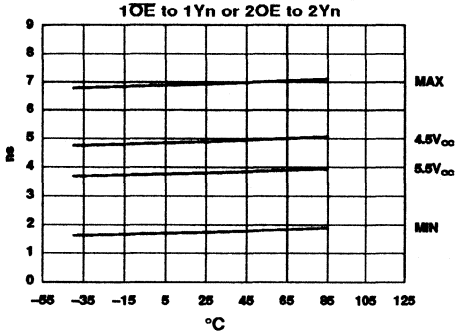
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$1\overline{OE}$ to 1Yn or 2OE to 2Yn



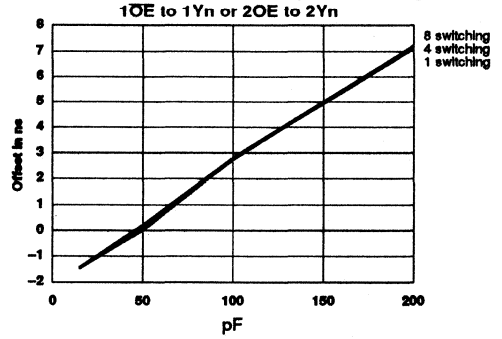
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$1\overline{OE}$ to 1Yn or 2OE to 2Yn



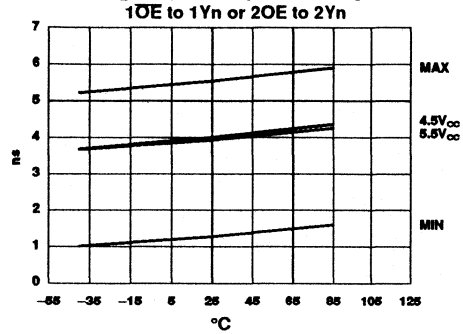
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$1\overline{OE}$ to 1Yn or 2OE to 2Yn



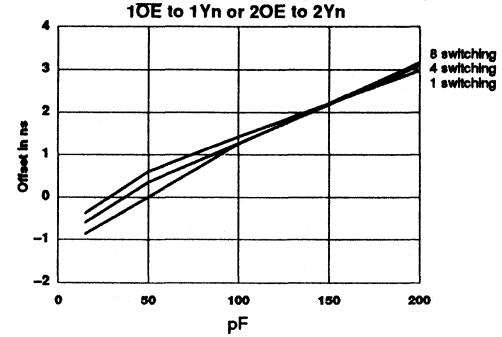
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$1\overline{OE}$ to 1Yn or 2OE to 2Yn



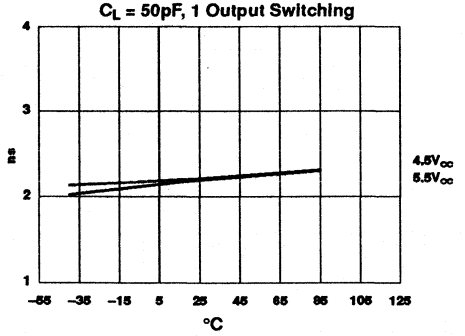
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$1\overline{OE}$ to 1Yn or 2OE to 2Yn



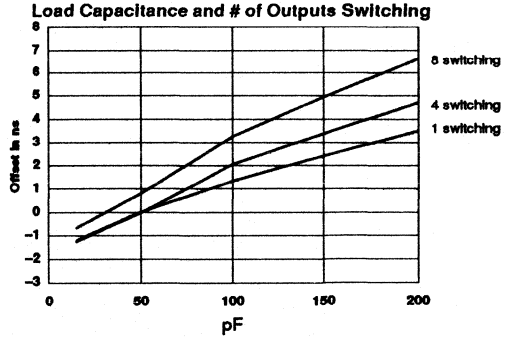
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$1\overline{OE}$ to 1Yn or 2OE to 2Yn



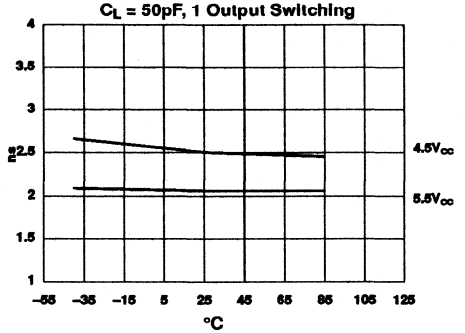
t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



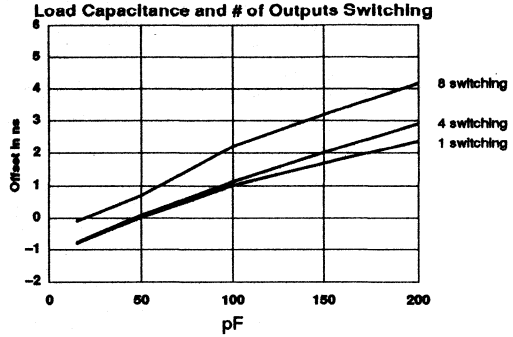
Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching



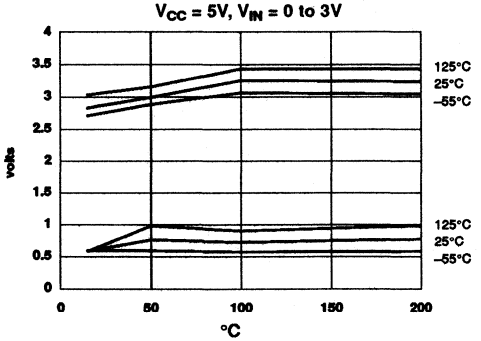
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



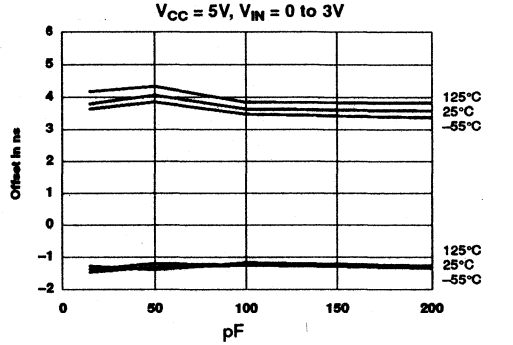
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching



V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



Octal buffer/line driver (3–State) 74ABT244

FEATURES

- Octal bus interface
- 3–State buffers
- Output capability: +64 mA/–32mA
- Latch–up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT244 high–performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT244 device is an octal buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3–State outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Ouputs disabled; V_{CC} =5.5V	500	nA

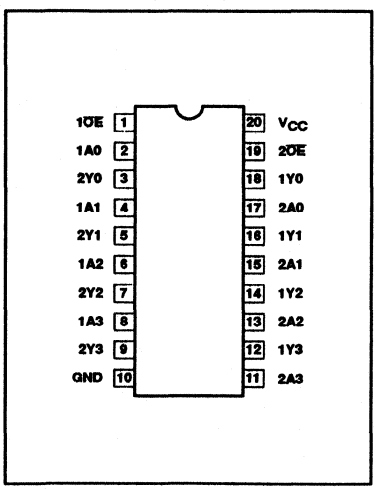
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20–pin plastic DIP	–40°C to +85°C	74ABT244N
20–pin plastic SOL	–40°C to +85°C	74ABT244D

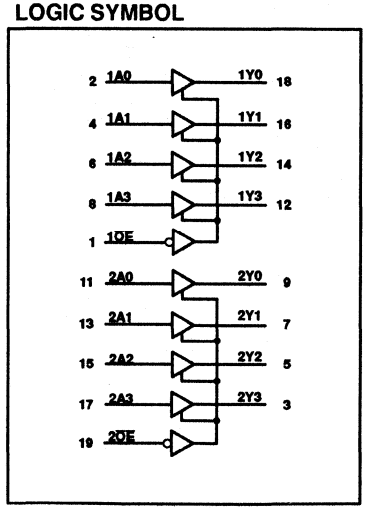
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11, 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	1Y0 – 1Y3	Data outputs
9, 7, 5, 3	2Y0 – 2Y3	Data outputs
1, 19	$1\overline{OE}$, $2\overline{OE}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

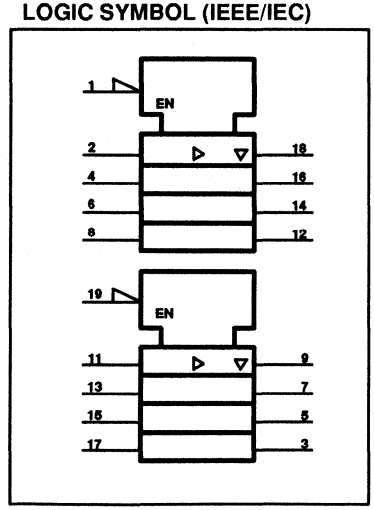
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS				OUTPUTS	
$1\overline{OE}$	1An	$2\overline{OE}$	2An	1Yn	1Yn
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1 Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
2. The performance capability of a high–performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3 The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		–32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	operating free–air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High–level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low–level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3–State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3–State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_O	Short–circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		0.5	mA
		Outputs 3–State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3–State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		0.5	mA

NOTES:
1 Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2 This is the increase in supply current for each input at 3.4V.

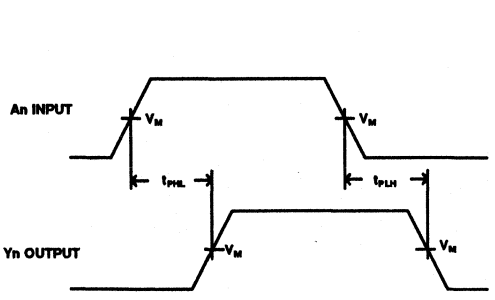
AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500Ω

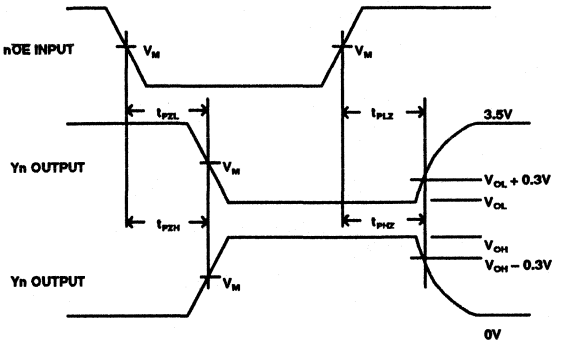
SYMBOL	PARAMETER	WAVEFORM	74ABT244					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = –40°C to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Yn	1	1.0 1.0	2.6 2.9	4.1 4.2	1.0 1.0	4.6 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 2.1	3.1 4.1	4.6 5.6	1.1 2.1	5.1 6.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.1 1.7	4.1 3.7	5.6 5.2	2.1 1.7	6.6 5.7	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

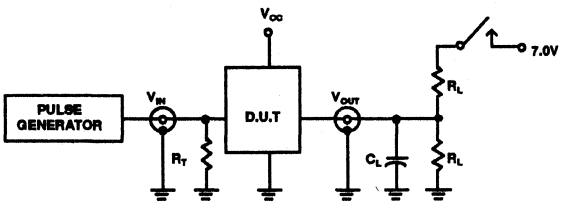


Waveform 1. Waveforms Showing the Input (An) to Output (Yn) Propagation Delays

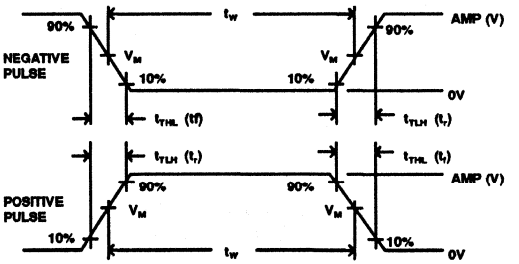


Waveform 2. Waveforms Showing the 3–State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3–State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

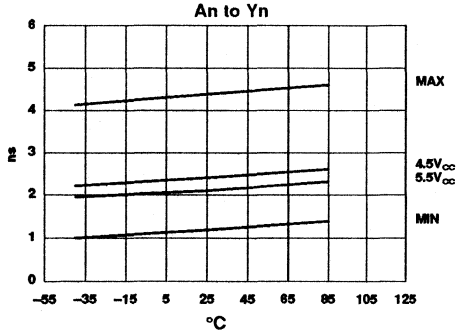
R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

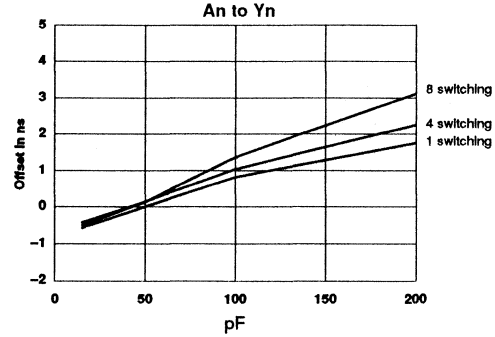
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1Mhz	500ns	2.5ns	2.5ns

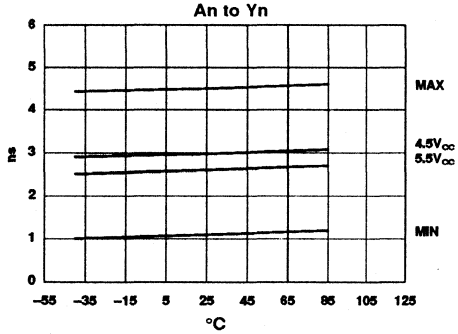
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
An to Yn



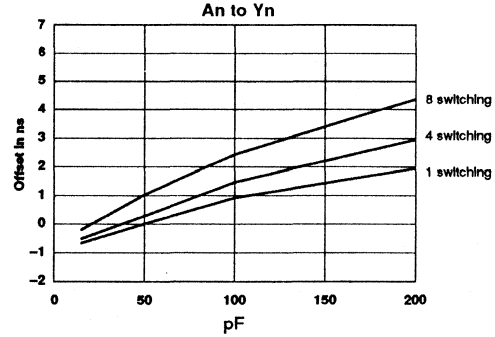
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
An to Yn



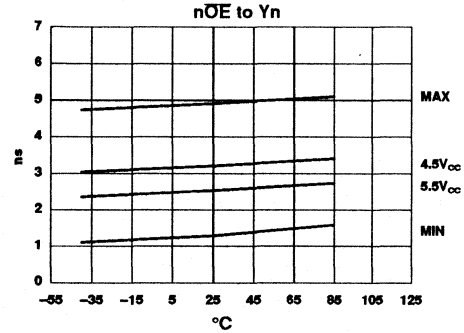
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
An to Yn



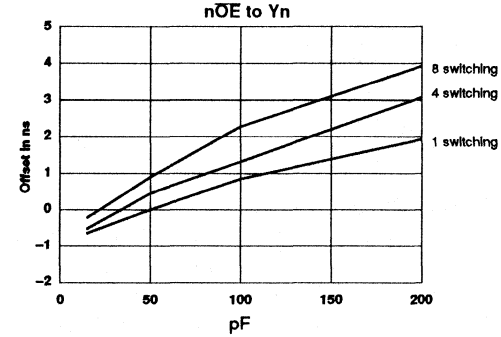
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
An to Yn



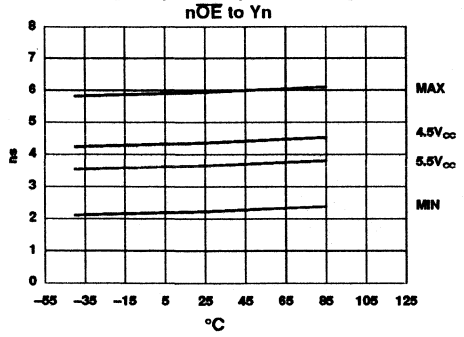
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nOE to Yn



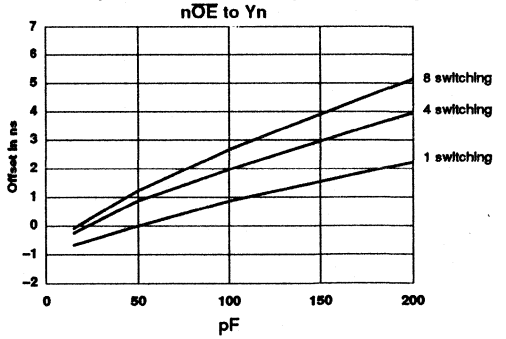
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
nOE to Yn



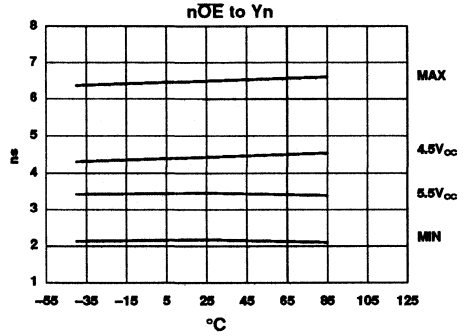
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$ to Yn



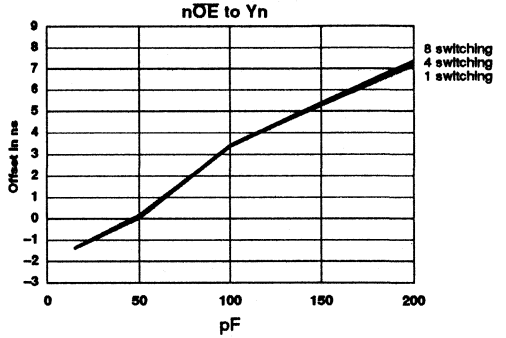
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to Yn



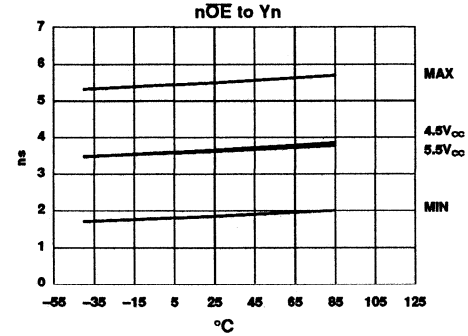
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$ to Yn



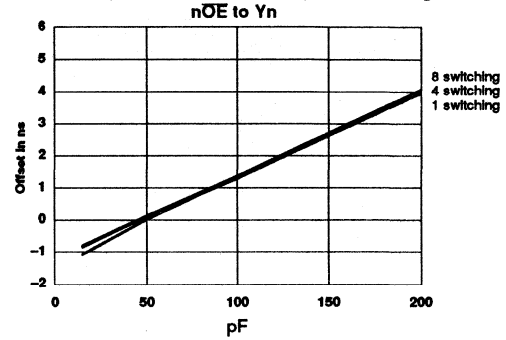
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to Yn



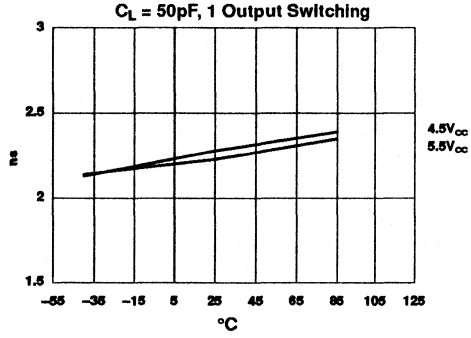
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$ to Yn



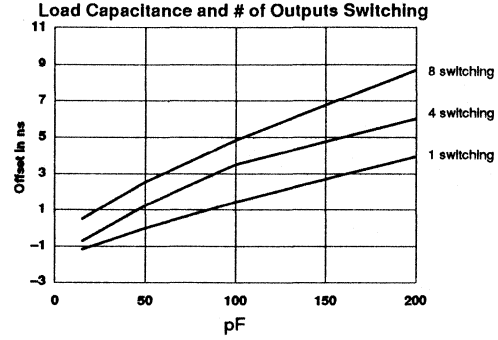
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to Yn



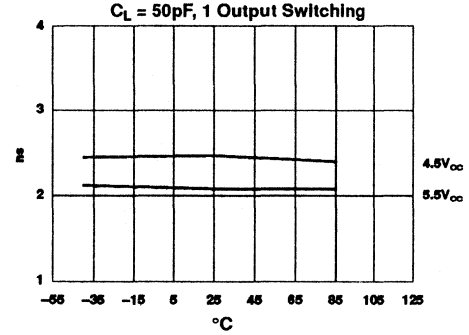
t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



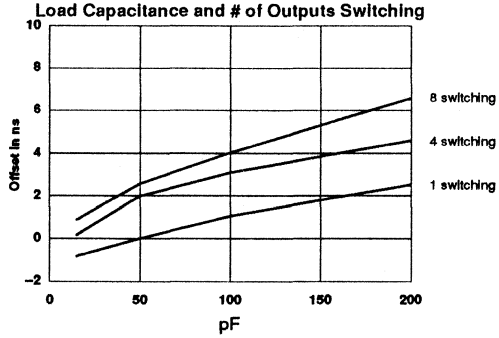
Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching



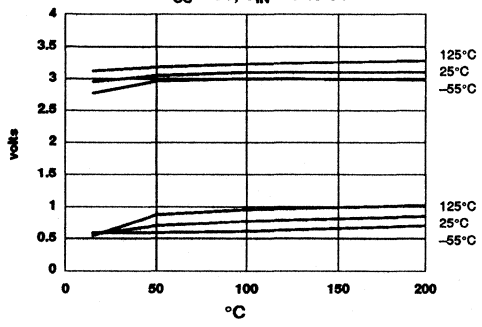
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



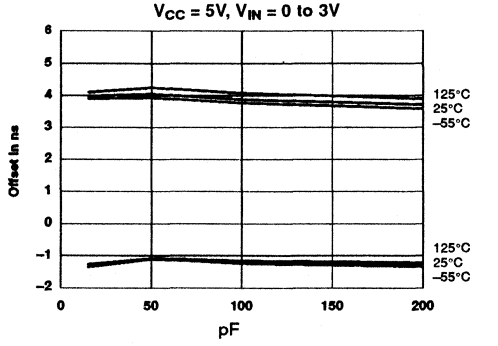
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching



V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



Octal transceiver with direction pin (3-State) — 74ABT245

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT245 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT245 device is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	An	Bn
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn, or Bn to An	C_L = 50pF; V_{CC} = 5V	2.9	ns
$C_{DIR, \overline{OE}}$	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O pin capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

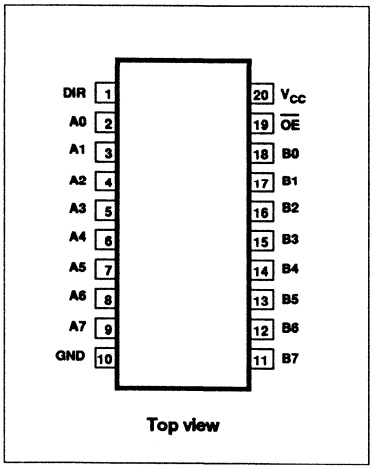
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT245N
20-pin plastic SOL	-40°C to +85°C	74ABT245D

PIN DESCRIPTION

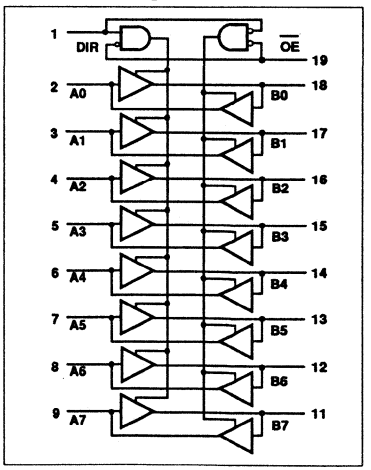
PIN NUMBER	SYMBOL	FUNCTION
1	DIR	Direction control input
2, 3, 4, 5 6, 7, 8, 9	A0 - A7	Data inputs/outputs (A side)
18, 17, 16, 15 14, 13, 12, 11	B0 - B7	Data inputs/outputs (B side)
19	$\overline{OE}$	Output enable
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

PIN CONFIGURATION

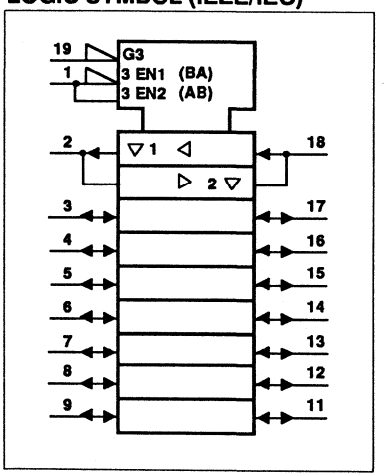


Top view

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
I_{IH} + I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
			Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
			Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

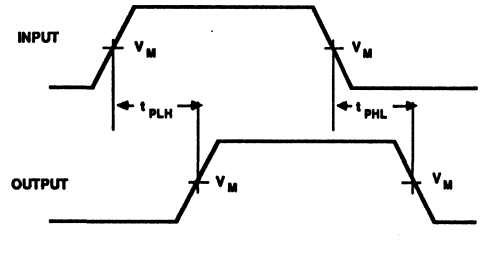
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

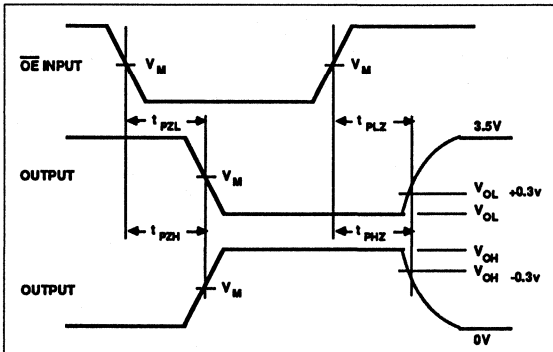
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.0 1.0	2.2 2.9	4.1 4.2	1.0 1.0	4.6 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.3 2.3	2.9 4.0	4.8 5.8	1.3 2.3	5.3 6.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.7 2.3	4.7 4.0	6.2 5.8	2.7 2.3	7.2 6.3	ns

AC WAVEFORMS

(V_M = 1.5V, V_{IN} = GND to 3.0V)

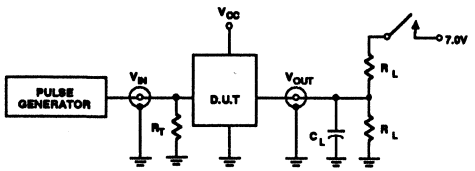


Waveform 1. Waveforms Showing the Input to Output Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

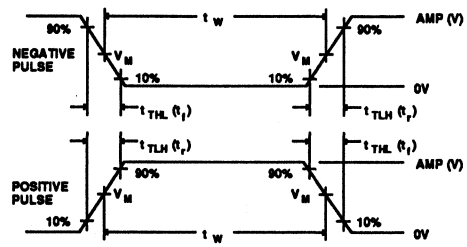
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

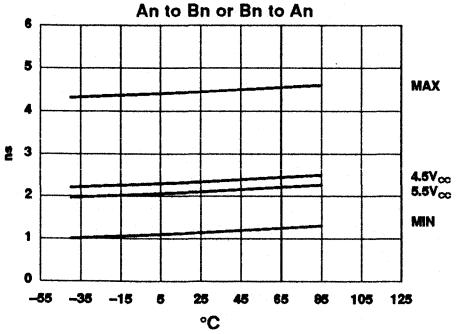


V_M = 1.5V

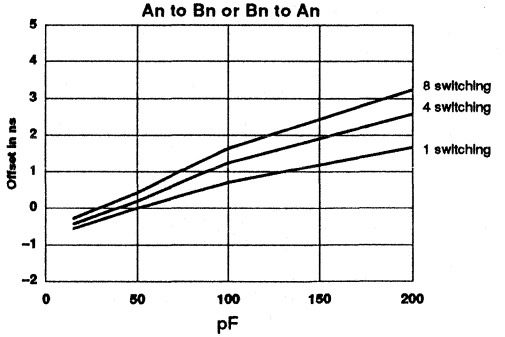
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

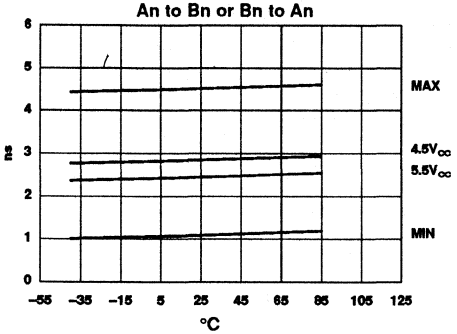
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
An to Bn or Bn to An



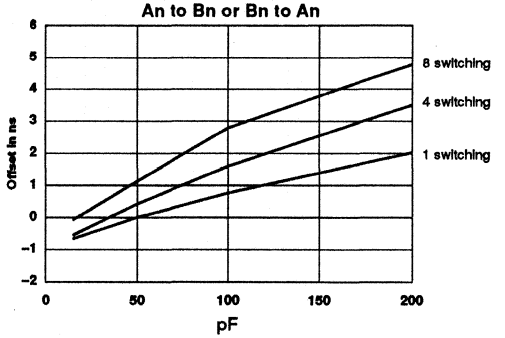
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
An to Bn or Bn to An



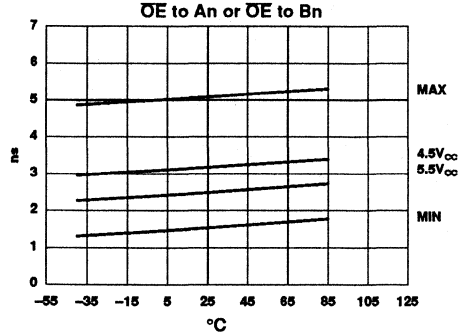
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
An to Bn or Bn to An



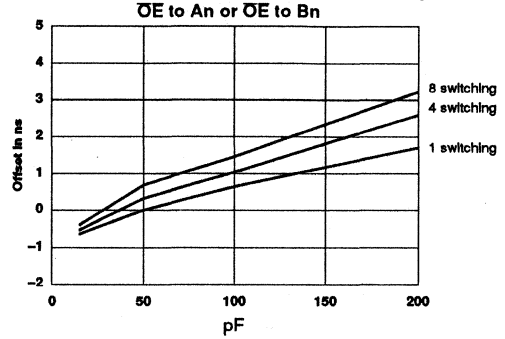
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
An to Bn or Bn to An



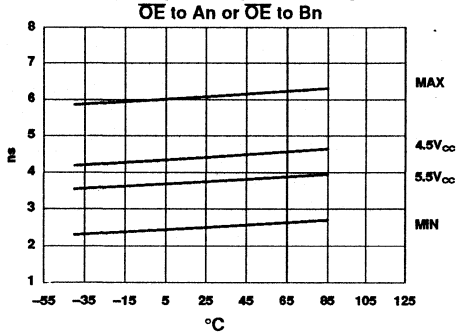
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



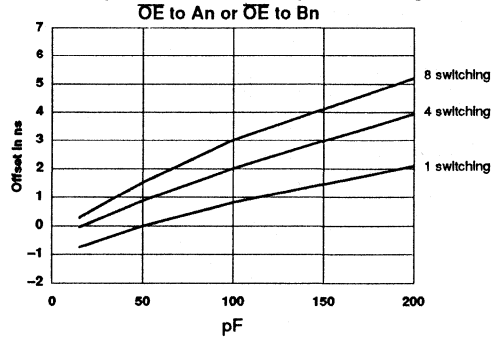
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



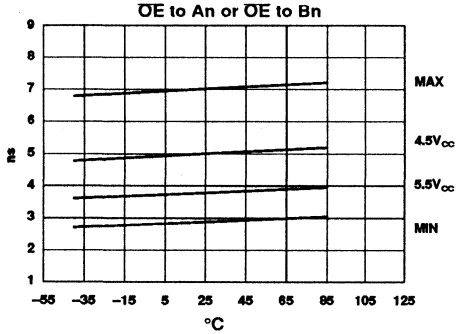
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



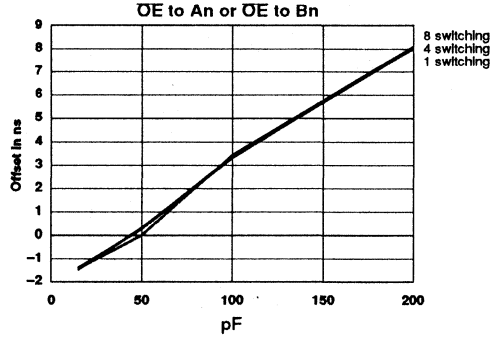
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



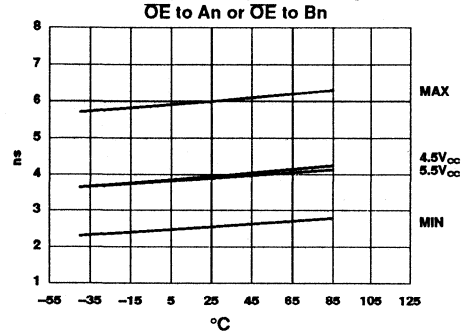
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



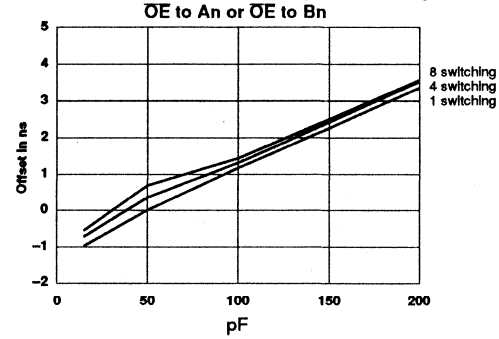
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



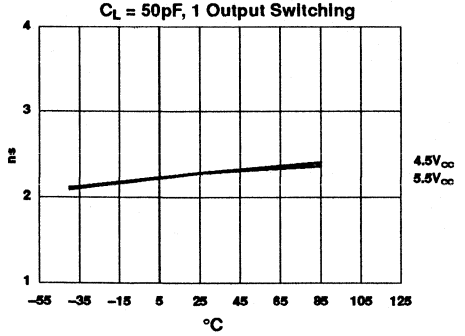
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



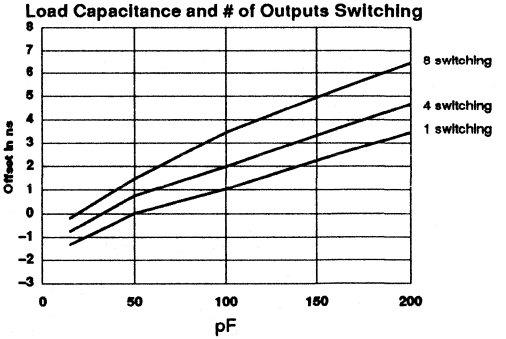
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



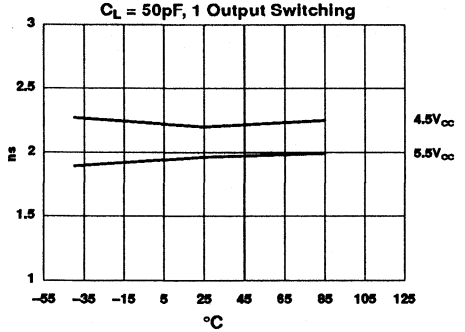
t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



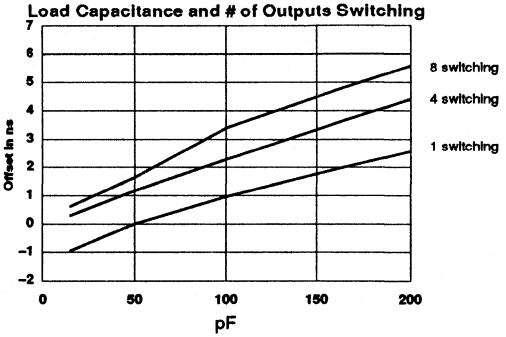
Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching



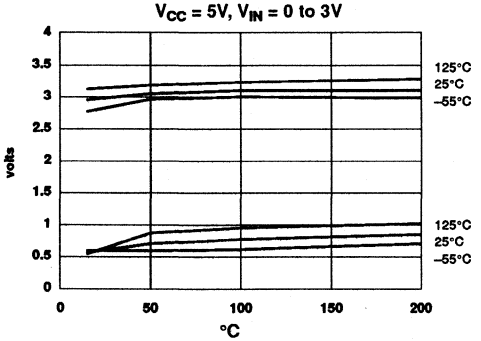
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



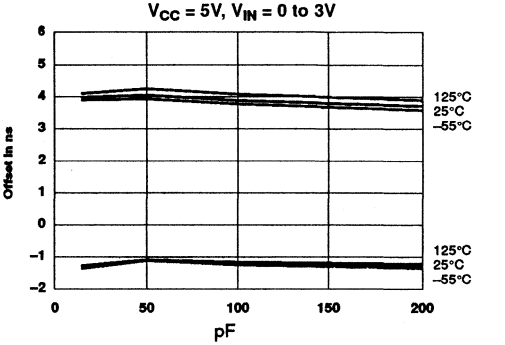
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching



V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



Octal D flip-flop

74ABT273

FEATURES

- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous Master Reset
- See 74ABT377 for clock enable version
- See 74ABT373 for transparent latch version
- See 74ABT374 for 3-State version

DESCRIPTION

The 74ABT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independent of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the CP and $\overline{MR}$ are common elements.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	5.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

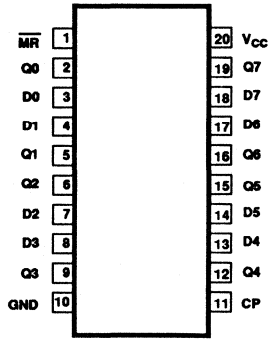
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT273N
20-pin plastic SOL	-40°C to +85°C	74ABT273D

PIN DESCRIPTION

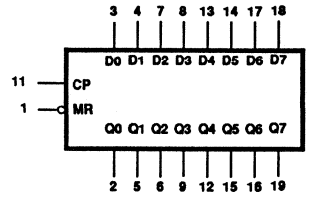
PIN NUMBER	SYMBOL	NAME AND FUNCTION
11	CP	Clock Pulse input (active rising edge)
3, 4, 7, 8 13, 14, 17, 18	D0 - D7	Data inputs
2, 5, 6, 9 12, 15, 16, 19	Q0 - Q7	Data outputs
1	$\overline{MR}$	Master Reset input (active-Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

PIN CONFIGURATION



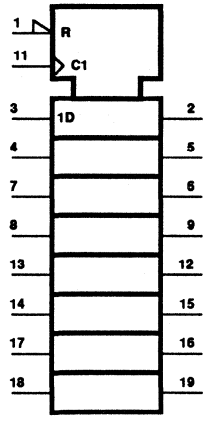
Top View

LOGIC SYMBOL



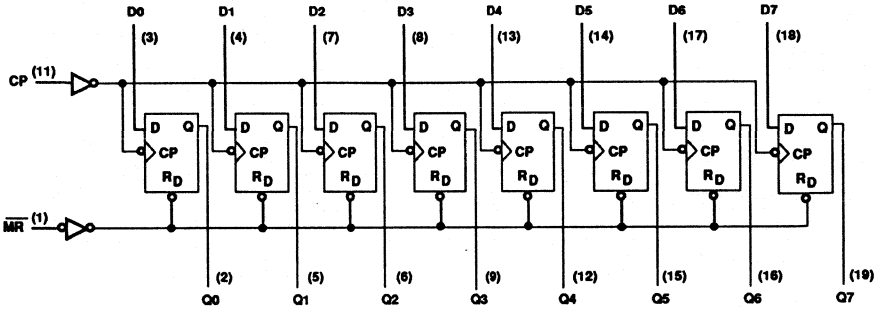
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)



Octal D flip-flop | 74ABT273

LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{MR}$	CP	D_n	Q0 - Q7	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

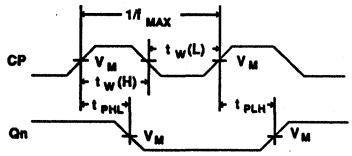
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40° C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	150	200		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	Waveform 1	2.5 3.3	4.5 5.3	6.0 6.8	2.5 3.3	6.5 7.3	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	Waveform 2	2.5	4.5	6.0	2.5	7.0	ns

AC SETUP REQUIREMENTS

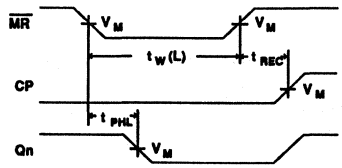
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40° C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CP	Waveform 3	2.0 2.5			2.0 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	Waveform 3	0.7 0.7			0.7 0.7		ns
$t_w(H)$ $t_w(L)$	Clock Pulse width High or Low	Waveform 1	3.3 3.3			3.3 3.3		ns
$t_w(L)$	Master Reset Pulse width, Low	Waveform 2	3.3			3.3		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	2.0			2.0		ns

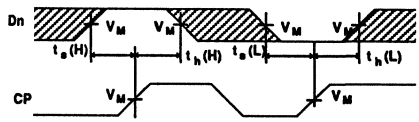
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

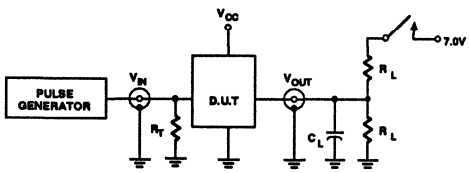


Waveform 3. Data Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

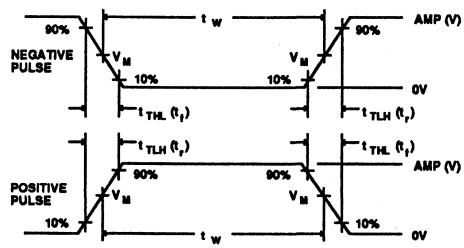
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

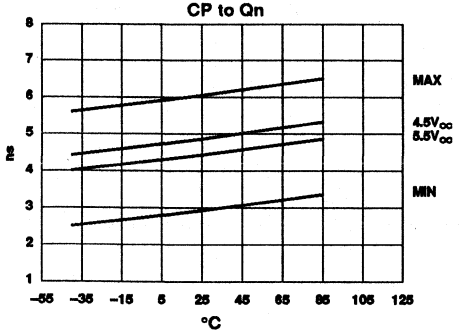


V_M = 1.5V

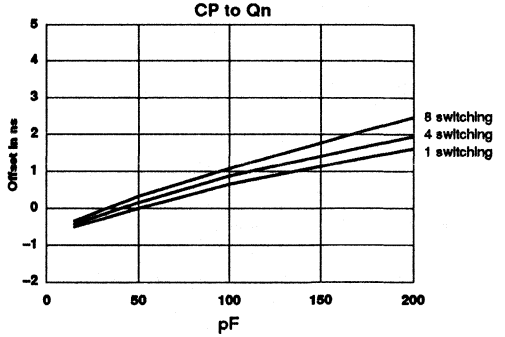
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

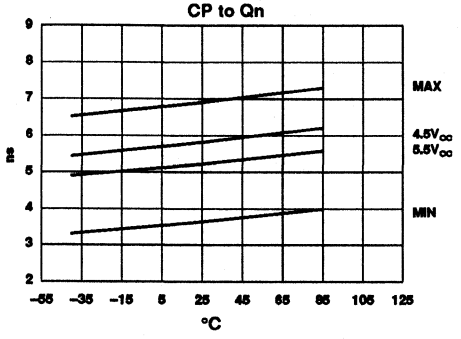
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
CP to Qn



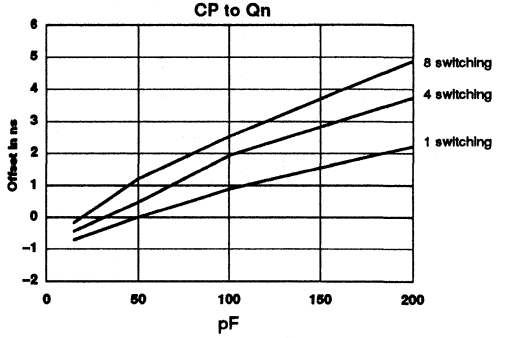
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
CP to Qn



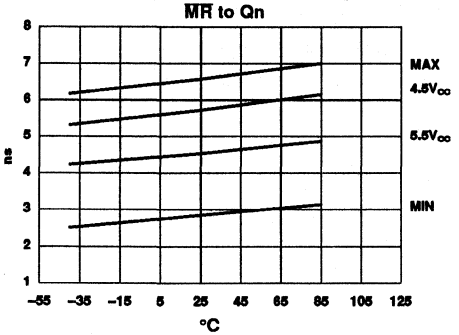
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
CP to Qn



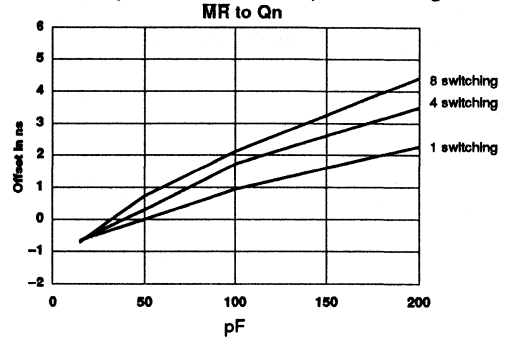
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
CP to Qn



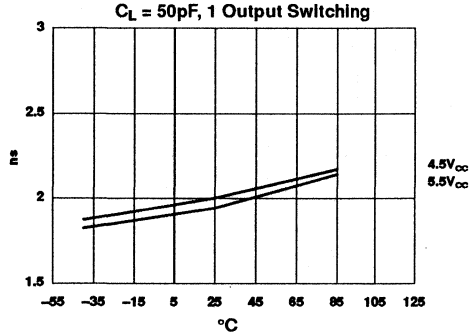
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{MR}$ to Qn



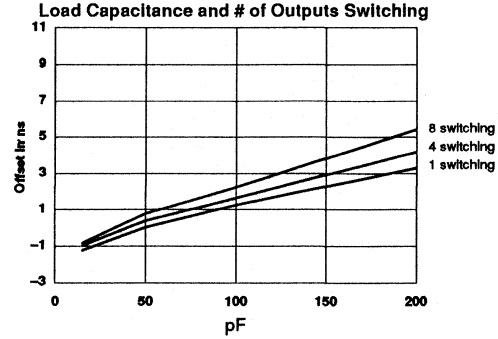
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
$\overline{MR}$ to Qn



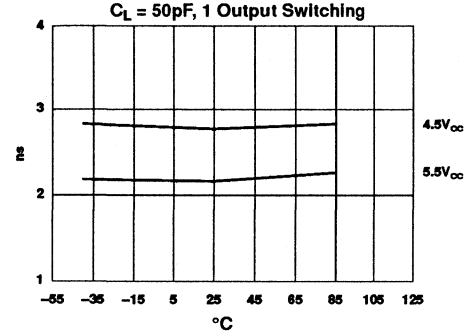
t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



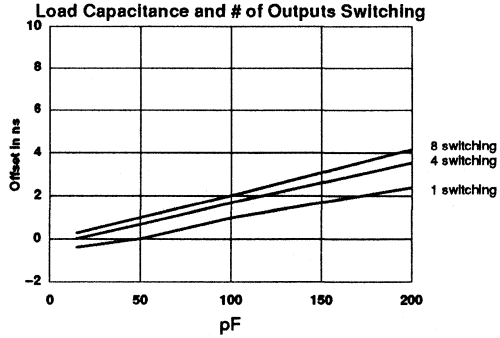
Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching



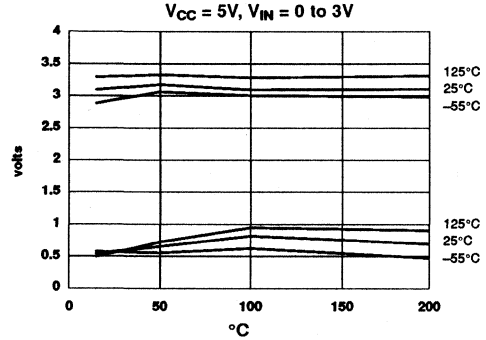
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



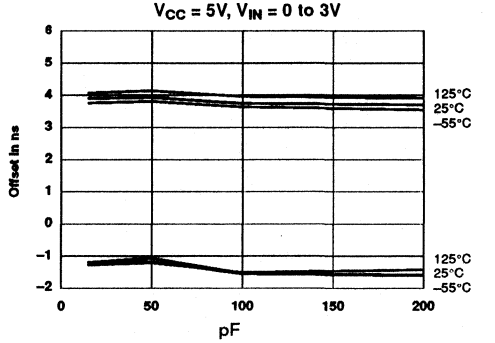
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching



V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



Octal D-type transparent latch (3-State) 74ABT373

FEATURES

- 8-bit transparent latch
- 3-State output buffers
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT373 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT373 device is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

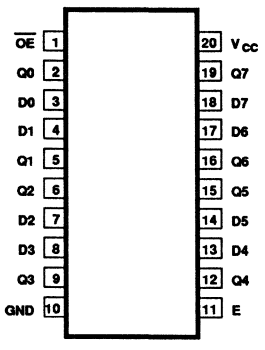
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50pF; V_{CC} = 5V	4.2	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

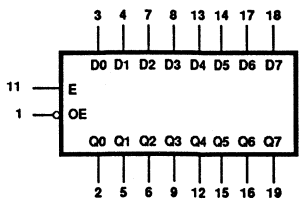
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT373N
20-pin plastic SOL	-40°C to +85°C	74ABT373D

PIN CONFIGURATION



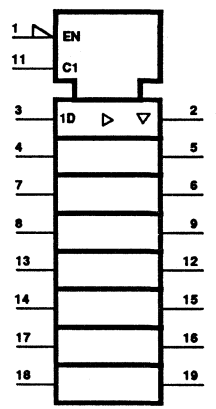
Top view

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)



Octal D-type transparent latch (3-State) 74ABT373

PIN DESCRIPTION

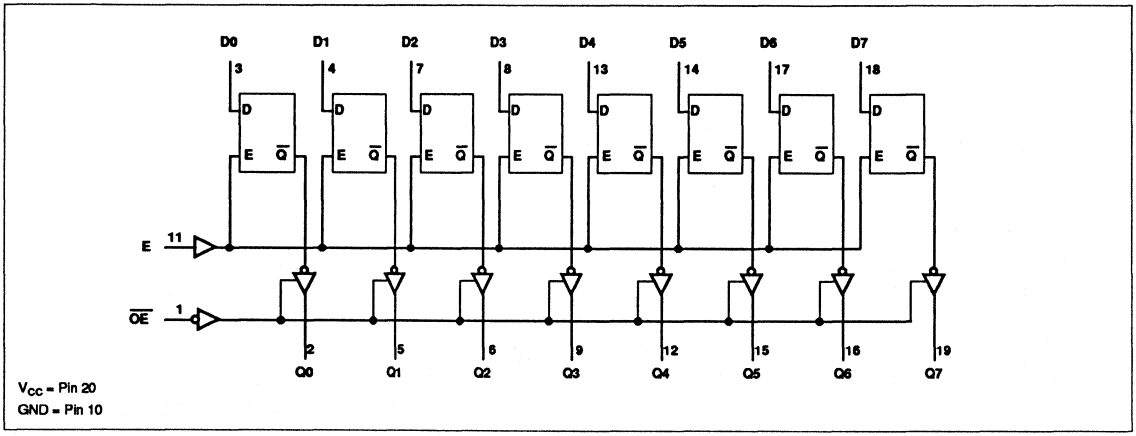
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output enable input (active Low)
3, 4, 7, 8, 13 14, 17, 18	Dn - Dn	Data inputs
2, 5, 6, 9, 12 15,16,19	Qn - Qn	3-State Outputs
11	E	Enable input (active High)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	Dn	REGISTER	Q0 - Q7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	Waveform 2	1.9 2.2	3.2 4.2	5.4 5.7	1.9 2.2	5.9 6.2	ns
t_{PLH} t_{PHL}	Propagation delay E to Qn	Waveform 1	2.6 3.2	4.0 5.2	6.1 6.7	2.2 3.2	6.6 7.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	Waveform 4 Waveform 5	1.2 2.7	3.2 4.7	4.7 6.2	1.2 2.7	5.2 6.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	Waveform 4 Waveform 5	2.5 2.0	4.9 4.2	6.4 6.0	2.5 2.0	6.9 6.5	ns

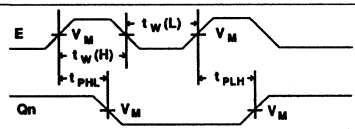
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

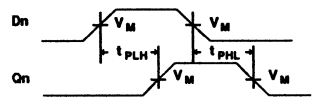
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time Dn to E	Waveform 3	1.9 1.5			1.9 1.5		ns
$t_h(H)$ $t_h(L)$	Hold time Dn to E	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_W(H)$	E pulse width, High or Low	Waveform 1	3.3			3.3		ns

AC WAVEFORMS

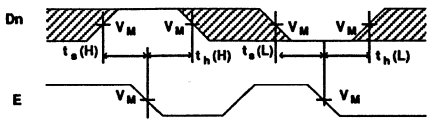
(V_M = 1.5V, V_{IN} = GND to 3.0V)



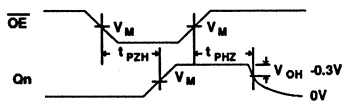
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width.



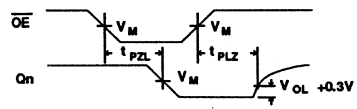
Waveform 2. Propagation Delay for Data to Outputs.



Waveform 3. Data Setup and Hold Times.



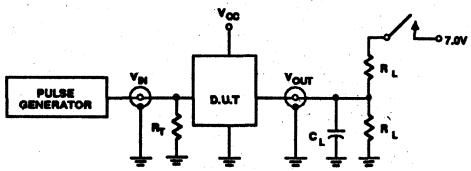
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time From High Level.



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level.

Octal D-type transparent latch (3-State) 74ABT373

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

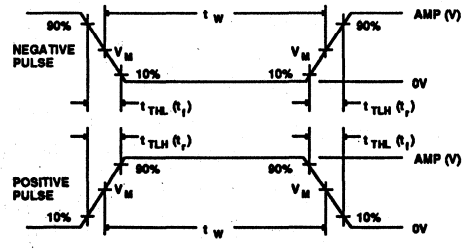
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

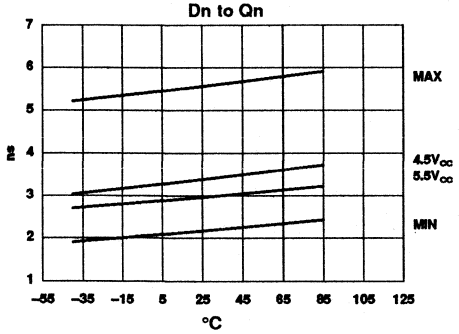


V_M = 1.5V

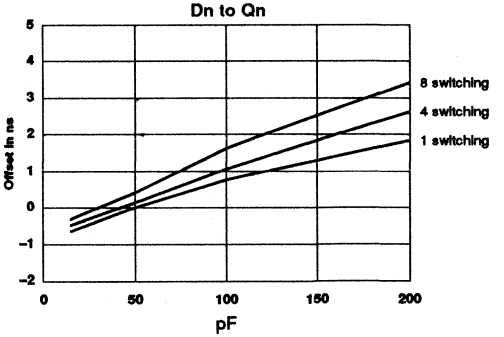
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

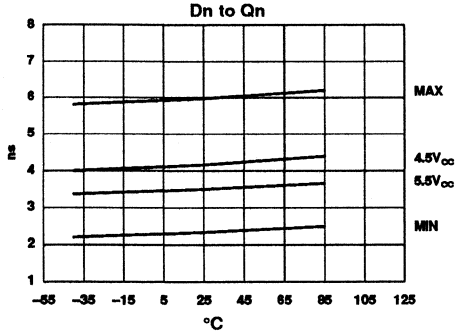
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
Dn to Qn



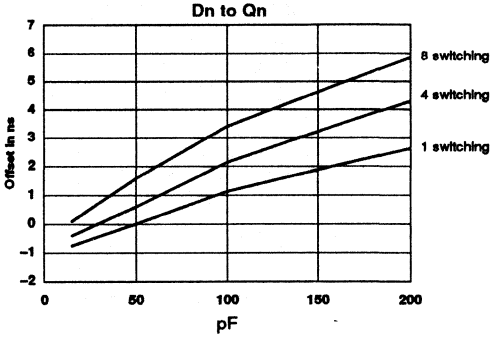
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
Dn to Qn



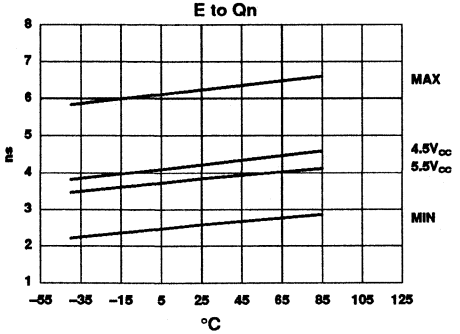
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
Dn to Qn



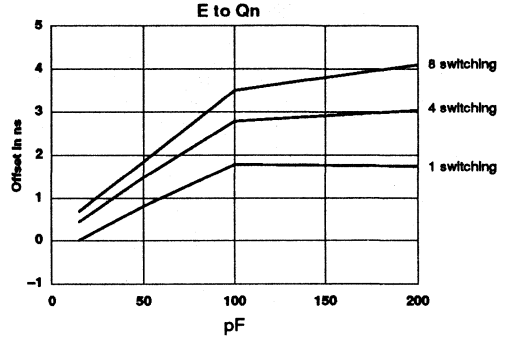
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
Dn to Qn



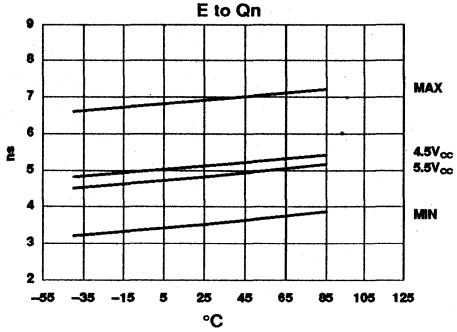
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
E to Qn



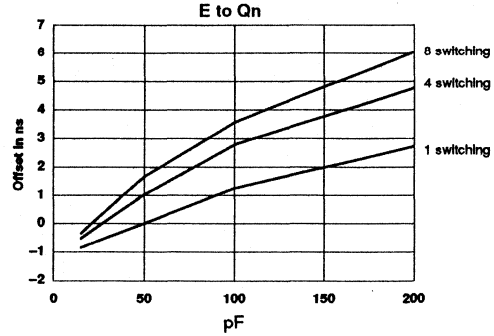
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
E to Qn



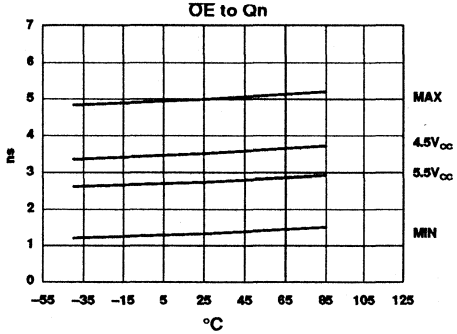
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
E to Qn



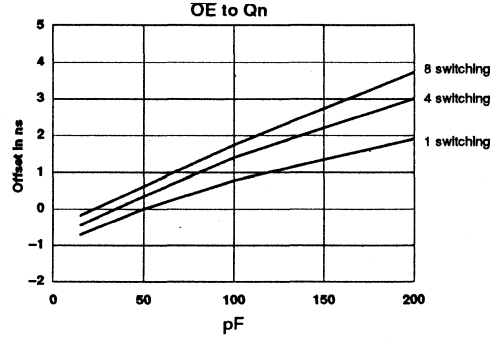
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
E to Qn



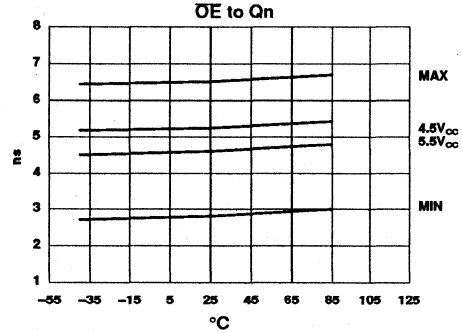
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to Qn



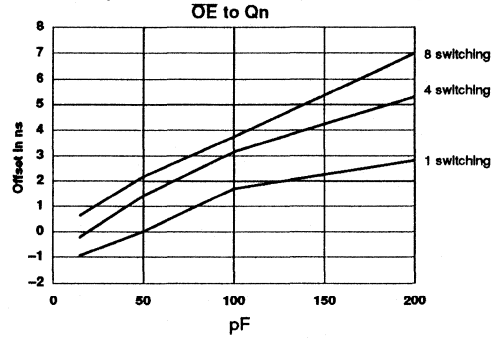
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to Qn



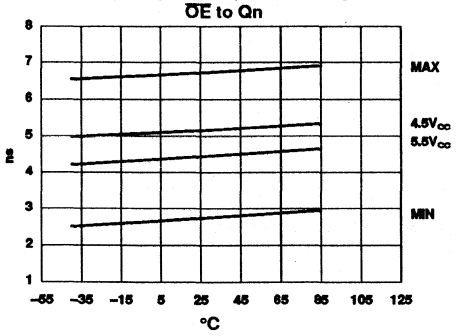
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to Qn



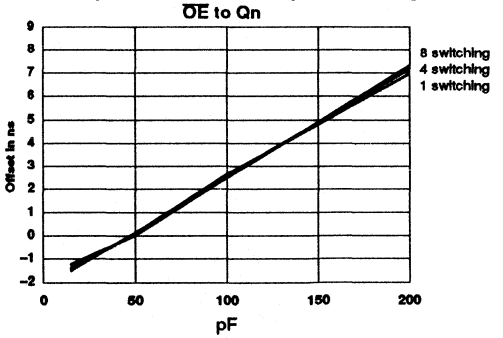
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to Qn



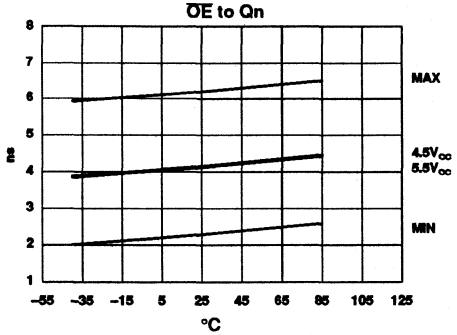
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to Qn



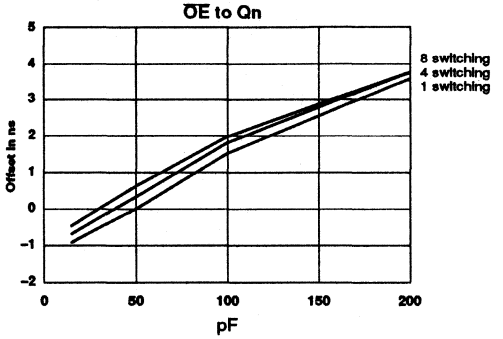
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to Qn



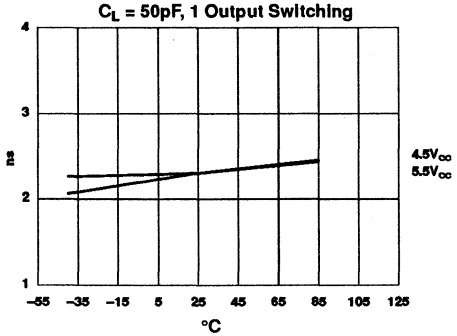
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to Qn



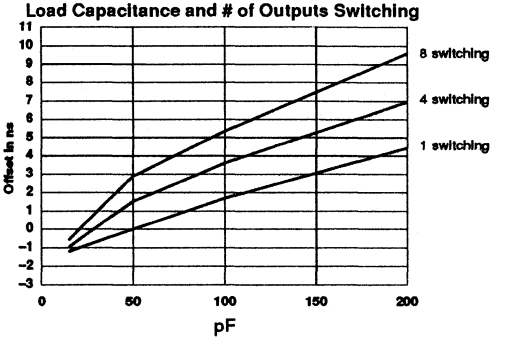
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to Qn

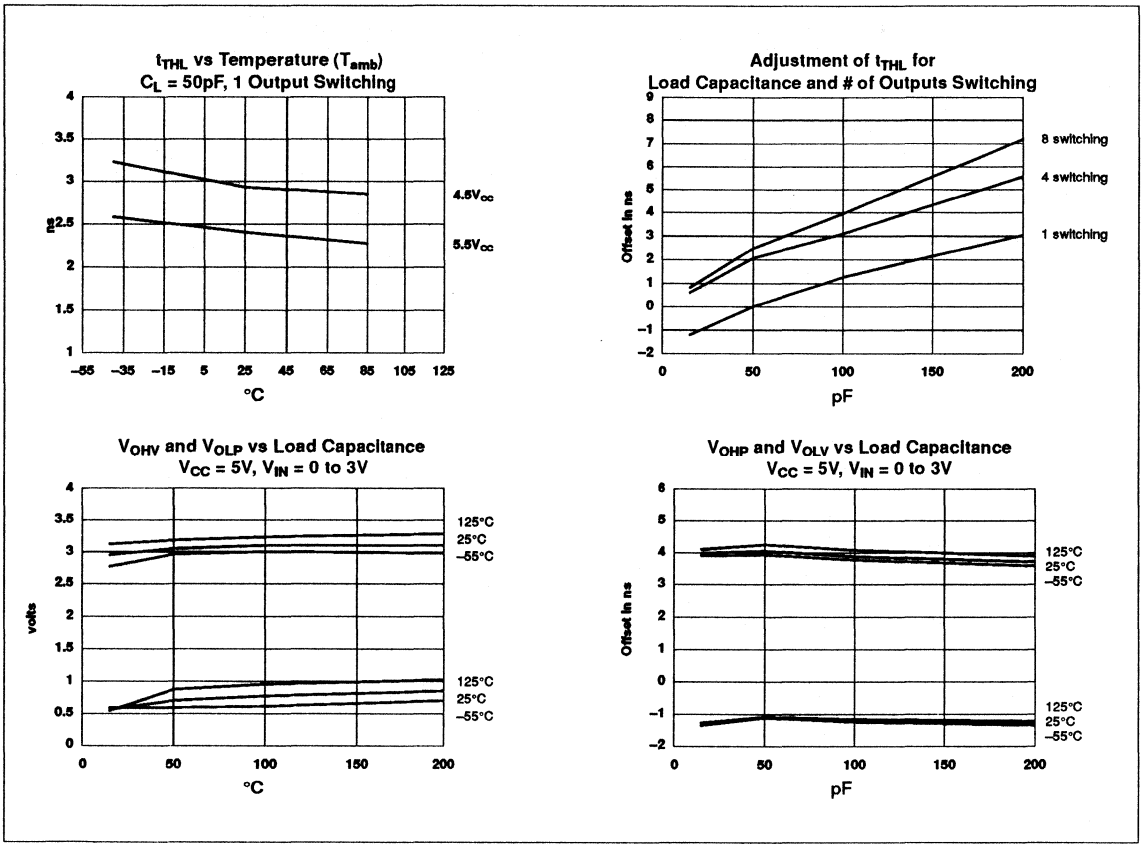


t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching




tTHL vs Temperature (Tamb)
CL = 50pF, 1 Output Switching
ns
4.5Vcc
5.5Vcc
°C
Adjustment of tTHL for
Load Capacitance and # of Outputs Switching
Offset in ns
8 switching
4 switching
1 switching
pF
VOHV and VOLP vs Load Capacitance
VCC = 5V, VIN = 0 to 3V
volts
125°C
25°C
–55°C
°C
VOHP and VOLV vs Load Capacitance
VCC = 5V, VIN = 0 to 3V
Offset in ns
125°C
25°C
–55°C
pF

Octal D-type flip-flop; positive-edge trigger (3-State) — 74ABT374

FEATURES

- 8-bit positive edge triggered register
- 3-State output buffers
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT374 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT374 is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	4.8	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

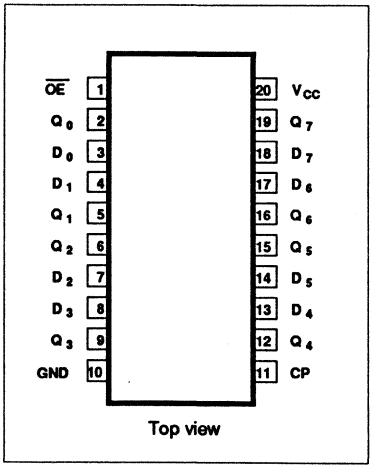
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT374N
20-pin plastic SOL	-40°C to +85°C	74ABT374D

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the clock operation.

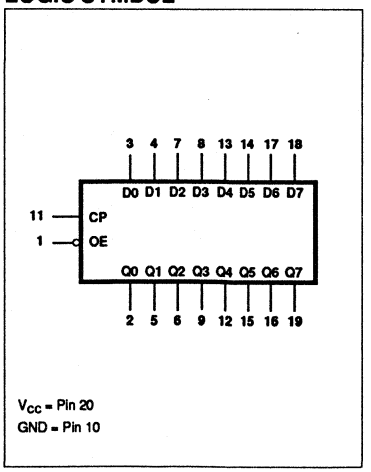
When $\overline{OE}$ is Low, the stored data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

PIN CONFIGURATION

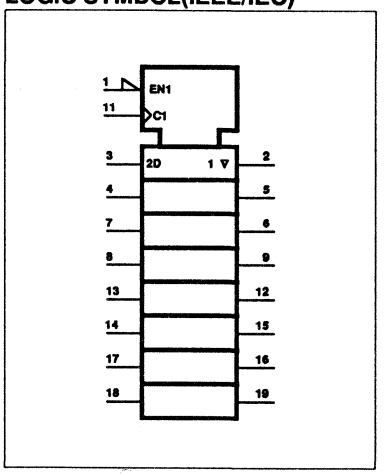


Top view

LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Octal D-type flip-flop; positive-edge trigger (3-State) 74ABT374

PIN DESCRIPTION

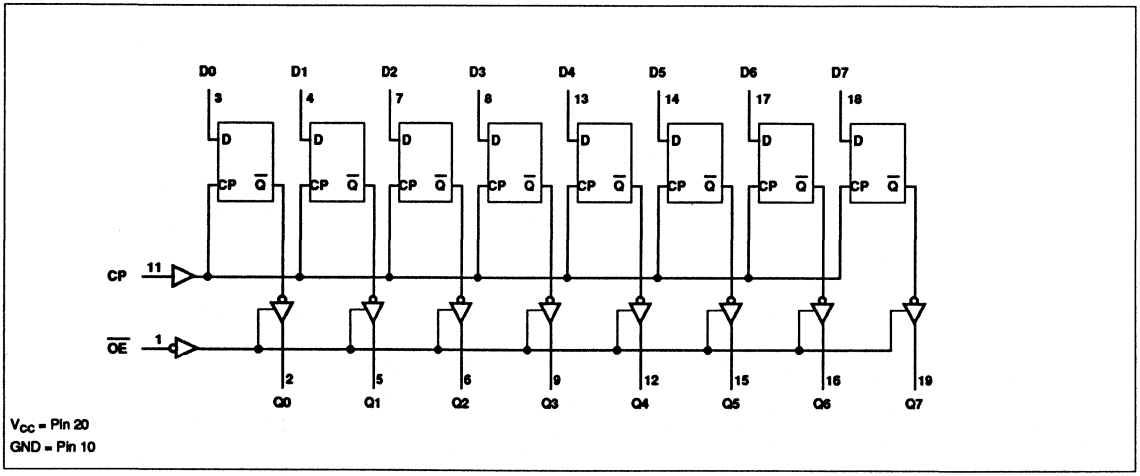
PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output Enable input (active Low)
3, 4, 7, 8, 13 14, 17, 18	D0 - D7	Data inputs
2, 5, 6, 9, 12 15, 16, 19	Q0 - Q7	Data outputs
11	CP	Clock Pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn	REGISTER	Q0 - Q7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↕	X	NC	NC	Hold
H H	↕ ↑	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = Not a Low-to-High clock transition

LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	150	200		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	Waveform 1	2.2 3.1	3.9 4.8	5.7 6.6	2.2 3.1	6.2 7.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	Waveform 3 Waveform 4	1.2 2.7	3.2 4.7	4.7 6.2	1.2 2.7	5.2 6.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	Waveform 3 Waveform 4	2.5 2.0	4.8 4.0	6.0 6.0	2.5 2.0	6.5 6.5	ns

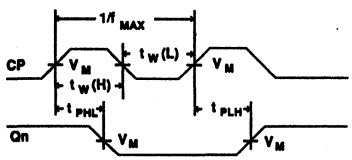
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

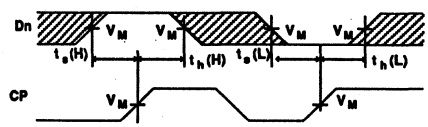
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ± 0.5V		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time Dn to CP	Waveform 2	1.0 1.5			1.0 1.5		ns
$t_h(H)$ $t_h(L)$	Hold time Dn to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_W(H)$	CP pulse width, High or Low	Waveform 1	3.3			3.3		ns

AC WAVEFORMS

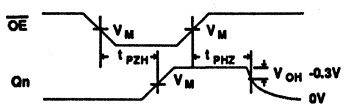
(V_M = 1.5V, V_{IN} = GND to 3.0V)



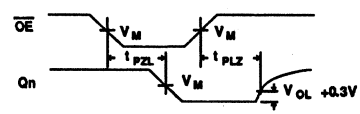
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup And Hold Times



Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level

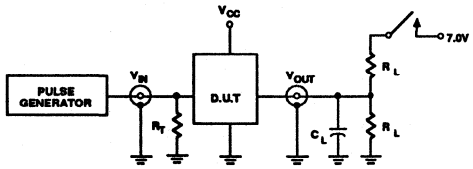


Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

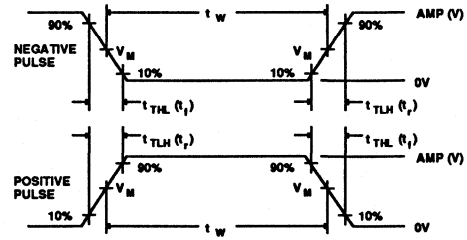
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

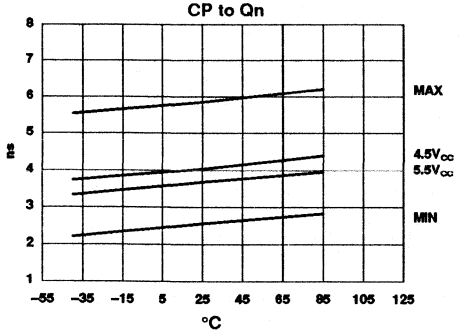


V_M = 1.5V

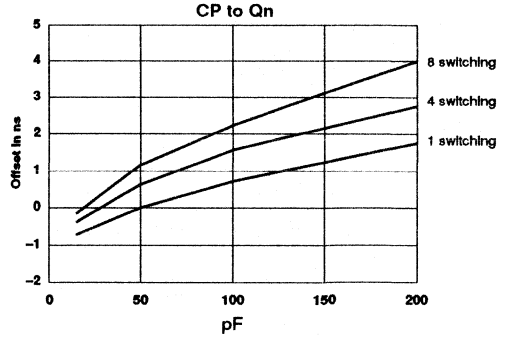
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

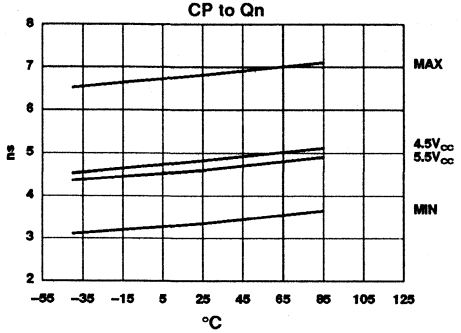
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
CP to Qn



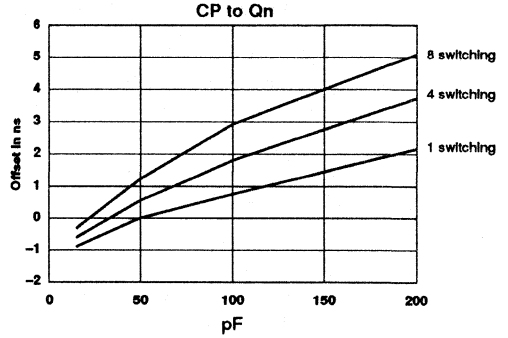
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
CP to Qn



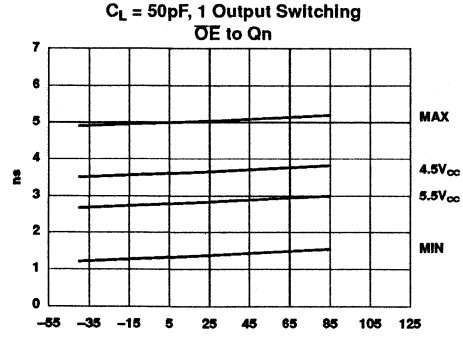
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
CP to Qn



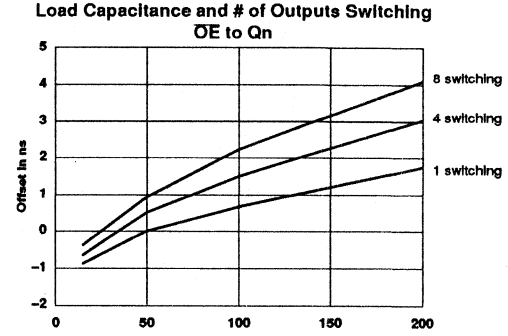
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
CP to Qn



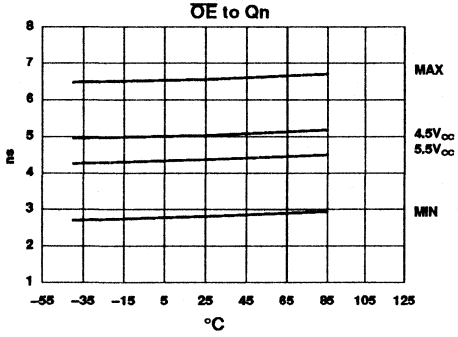
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to Qn



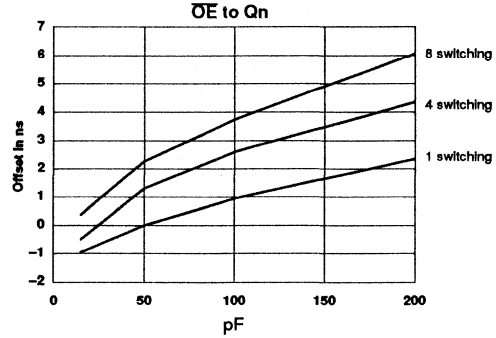
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to Qn



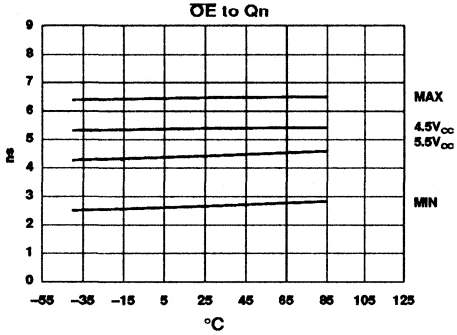
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to Qn



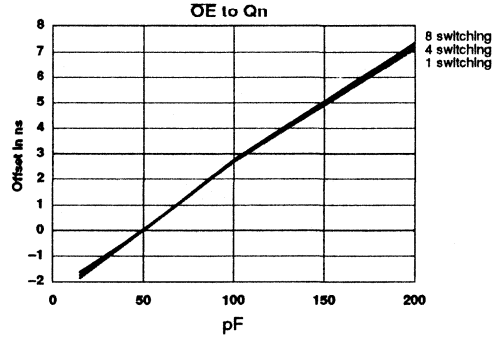
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to Qn



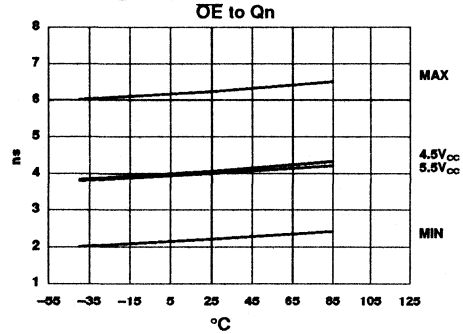
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to Qn



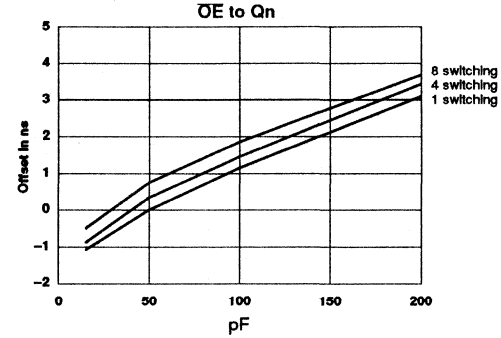
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to Qn



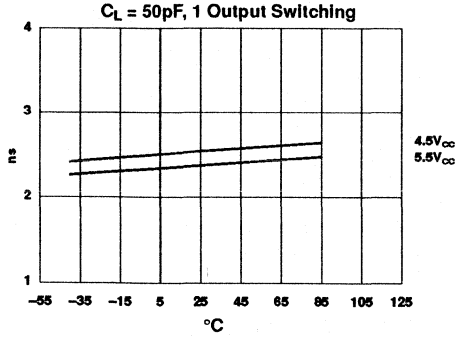
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to Qn



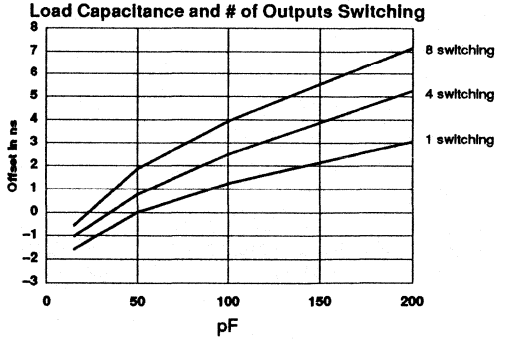
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to Qn



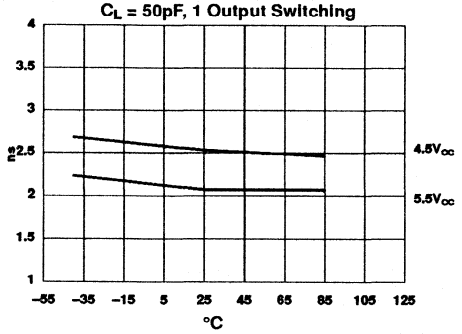
t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



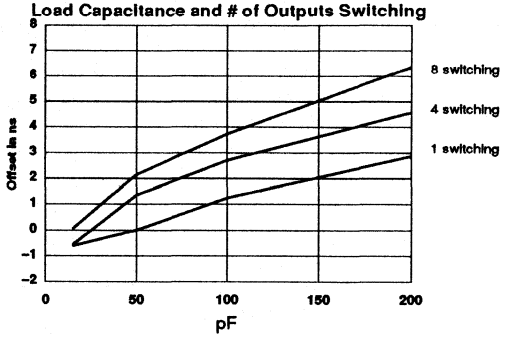
Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching



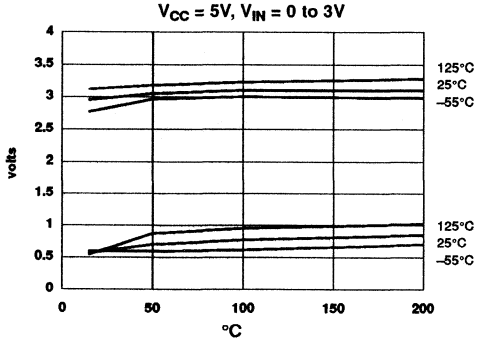
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



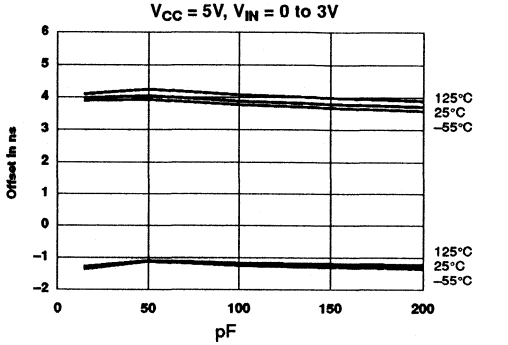
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching



V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



Octal D-type flip-flop with enable — 74ABT377

FEATURES

- Ideal for addressable register applications
- 8-bit positive edge triggered register
- Enable for address and data synchronization applications
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT377 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT377 has 8 edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) input loads all flip-flops simultaneously when the Enable ($\overline{E}$) input is Low.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The $\overline{E}$ input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	5.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

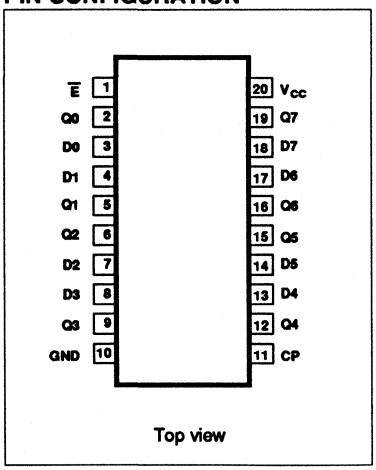
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT377N
20-pin plastic SOL	-40°C to +85°C	74ABT377D

PIN DESCRIPTION

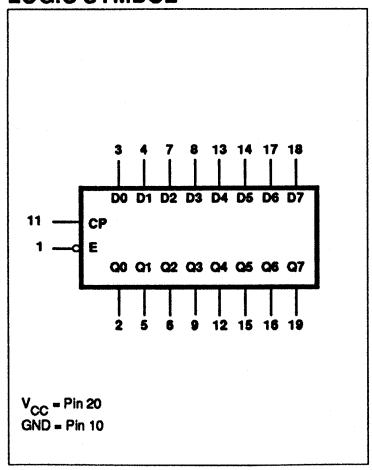
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{E}$	Enable input (active Low)
3, 4, 7, 8, 13 14, 17, 18	D0 - D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0 - Q7	Data outputs
11	CP	Clock Pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

PIN CONFIGURATION

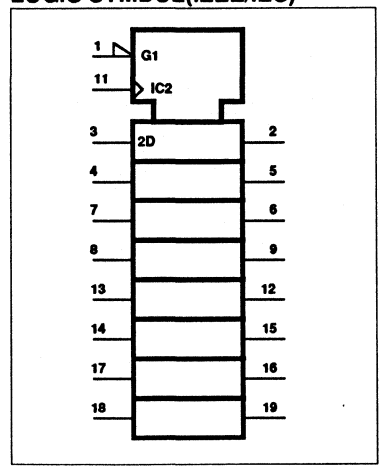


Top view

LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



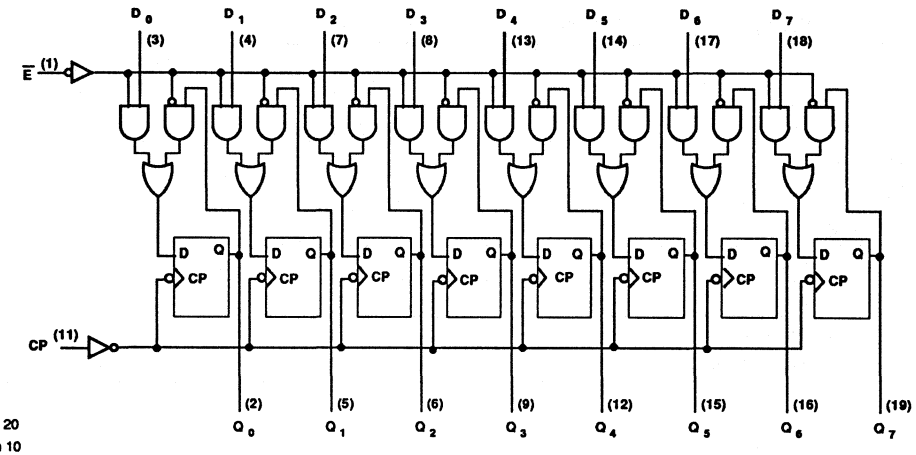
Octal D-type flip-flop with enable | 74ABT377

FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{E}$	CP	Dn	Qn	
l	↑	h	H	Load "1"
l	↑	l	L	Load "0"
h	↑	X	no change	Hold (do nothing)
H	X	X	no change	

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

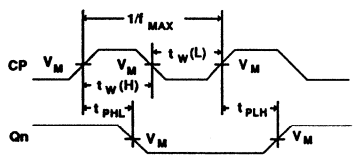
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	150	200		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	Waveform 1	2.2 3.1	4.5 5.3	6.0 6.8	2.2 3.1	6.5 7.3	ns

AC SETUP REQUIREMENTS

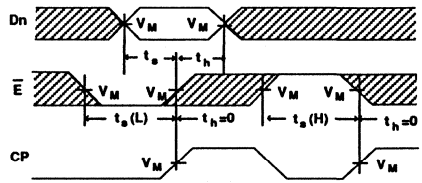
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CP	Waveform 2	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{E}$ to CP	Waveform 2	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{E}$ to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	Clock Pulse width High or Low	Waveform 1	3.3 3.3			3.3 3.3		ns

AC WAVEFORMS



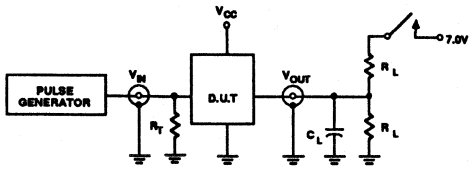
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data And Enable Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

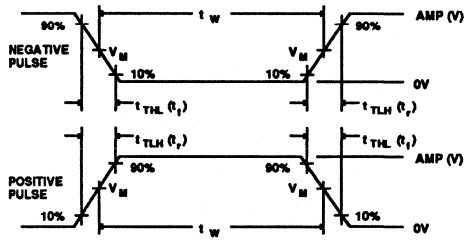
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

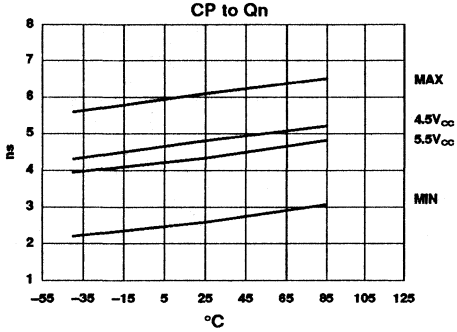


V_M = 1.5V

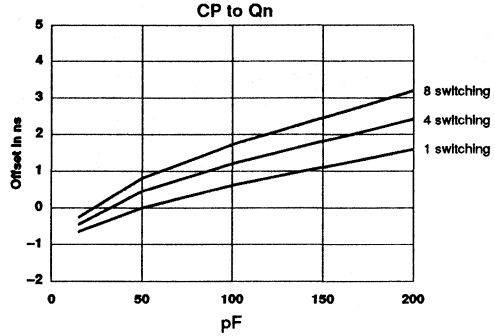
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

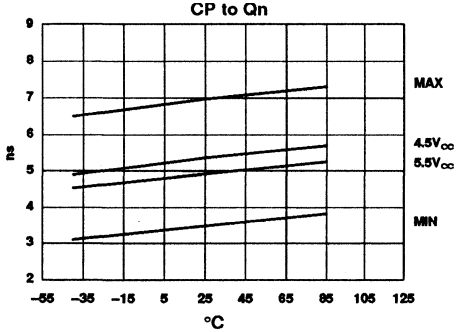
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
CP to Qn



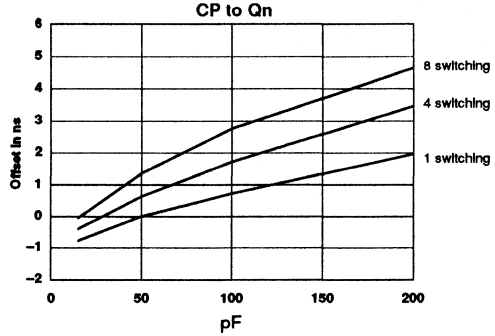
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
CP to Qn



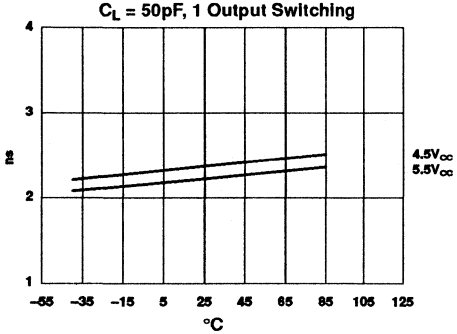
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
CP to Qn



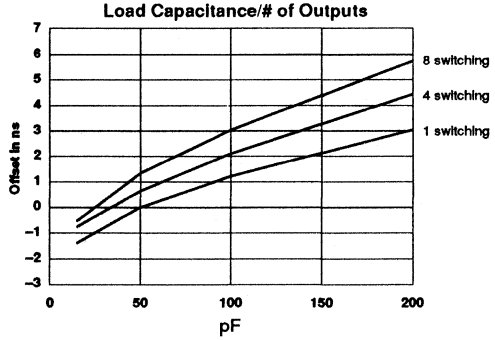
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
CP to Qn

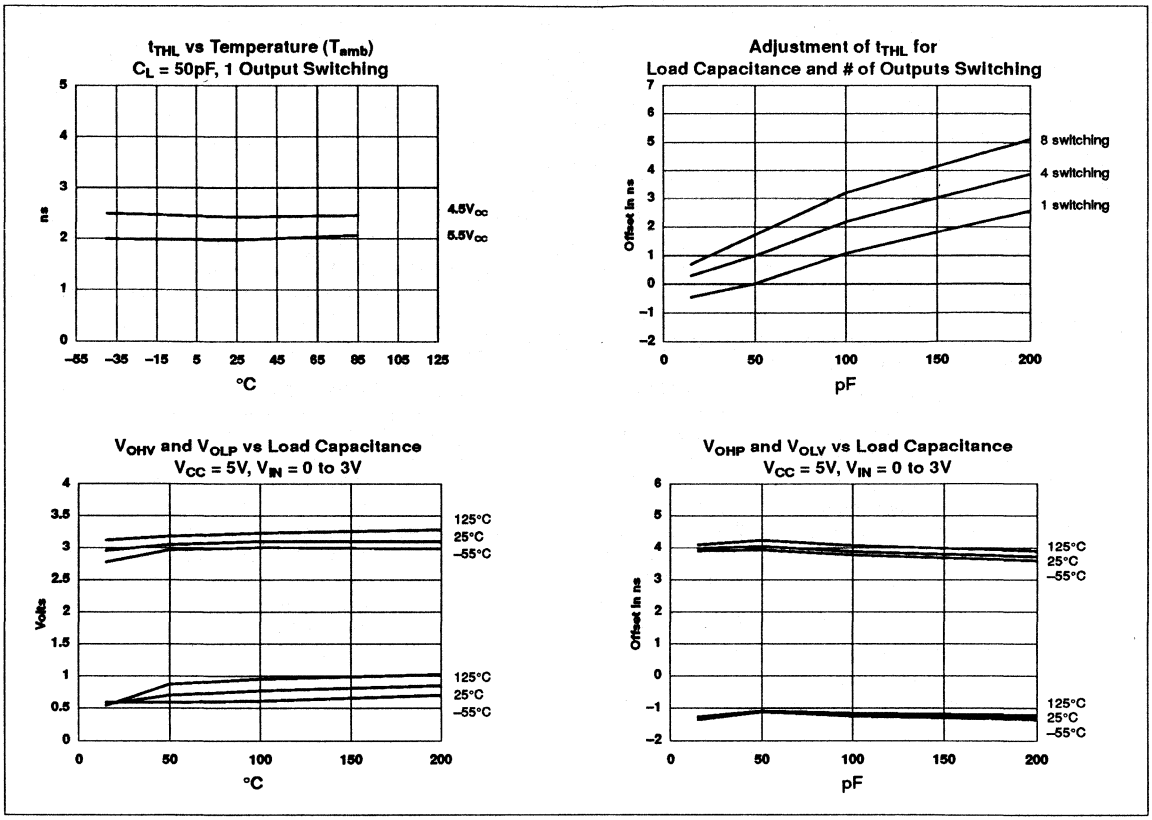


t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



Adjustment of t_{TLH} for
Load Capacitance/# of Outputs




t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V_{CC}
5.5V_{CC}
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
8 switching
4 switching
1 switching
V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
Volts
°C
125°C
25°C
–55°C
V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
Offset in ns
pF
125°C
25°C
–55°C

Octal D-type flip-flop, inverting (3-State) — 74ABT534

FEATURES

- 8-bit positive edge triggered register
- 3-State output buffers
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT534 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT534 is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is inverted and transferred to the corresponding flip-flop's output.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	6.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

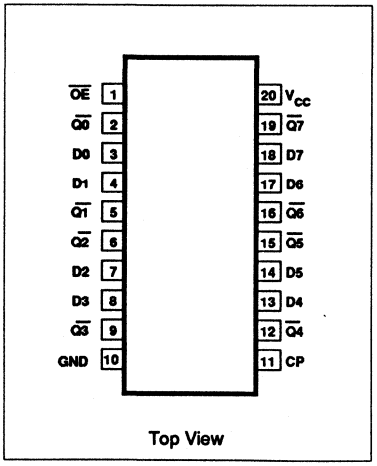
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT534N
20-pin plastic SOL	-40°C to +85°C	74ABT534D

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

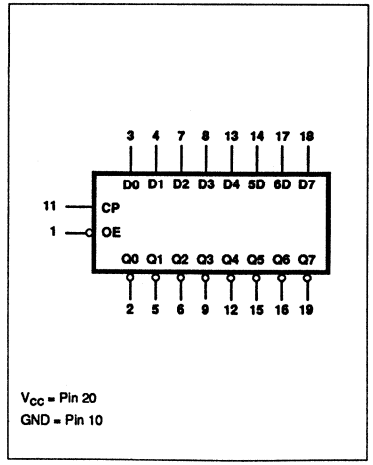
When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

PIN CONFIGURATION

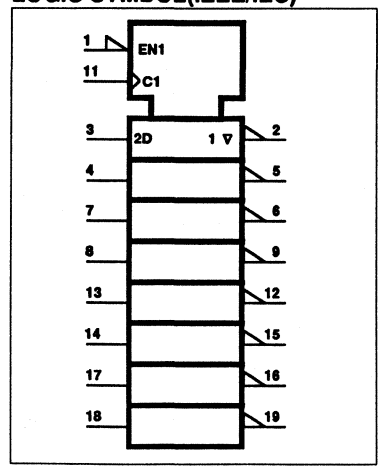


Top View

LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Octal D-type flip-flop, inverting (3-State) 74ABT534

PIN DESCRIPTION

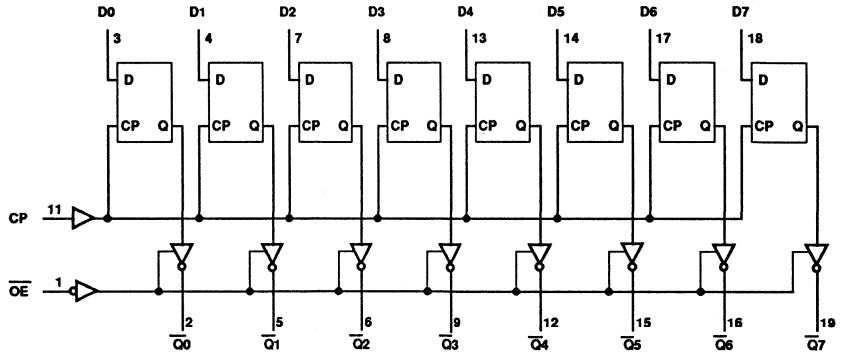
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output Enable input (active Low)
3, 4, 7, 8, 13 14, 17, 18	D0 - D7	Data inputs
2, 5, 6, 9, 12 15, 16, 19	$\overline{Q0}$ - $\overline{Q7}$	Inverting 3-State outputs
11	CP	Clock Pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn	REGISTER	$\overline{Q0}$ - $\overline{Q7}$	
L L	↑ ↑	l h	L H	H L	Load and read register
L	↕	X	NC	NC	Hold
H H	↕ ↑	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = Not a Low-to-High clock transition

LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Octal D-type flip-flop, inverting (3-State) 74ABT534

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40° C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	125	175		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}$n	Waveform 1	2.6 3.4	5.1 6.0	5.9 6.7	2.6 3.4	6.7 7.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	Waveform 3 Waveform 4	1.0 2.6	3.3 5.0	4.2 5.8	1.0 2.6	5.0 6.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	Waveform 3 Waveform 4	2.4 2.3	5.3 5.1	6.6 5.8	2.4 2.3	7.3 6.5	ns

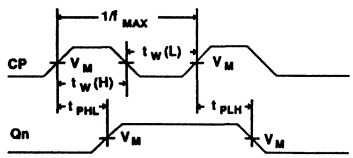
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

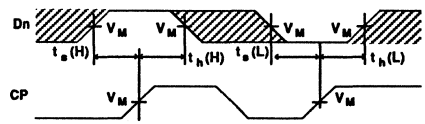
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40° C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Set-up time Dn to CP	Waveform 2	1.6 2.2			1.6 2.2		ns
t_h(H) t_h(L)	Hold time Dn to CP	Waveform 2	0.5 0.5			0.5 0.5		ns
t_W(H)	CP pulse width, High or Low	Waveform 1	3.5 3.5			3.5 3.5		ns

AC WAVEFORMS

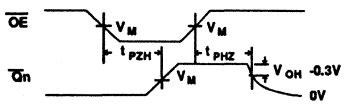
(V_M = 1.5V, V_{IN} = GND to 3.0V)



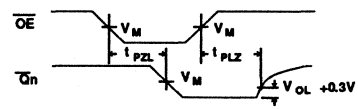
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup And Hold Times



Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



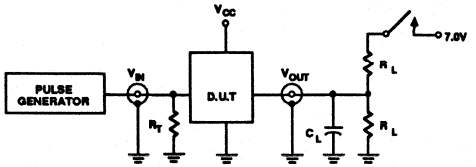
Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.

Octal D-type flip-flop, inverting (3-State) 74ABT534

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

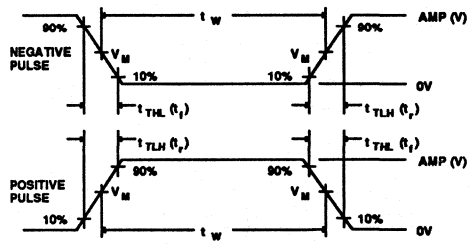
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

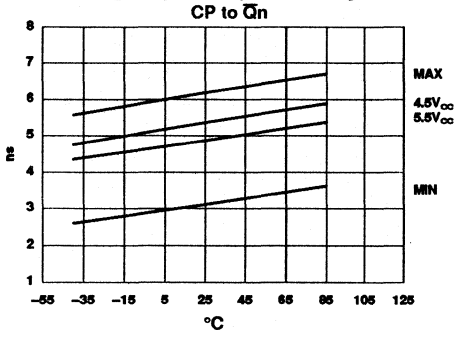


V_M = 1.5V

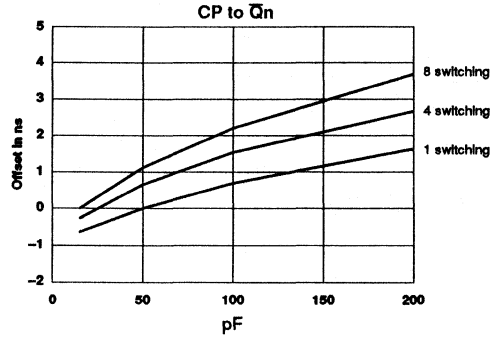
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

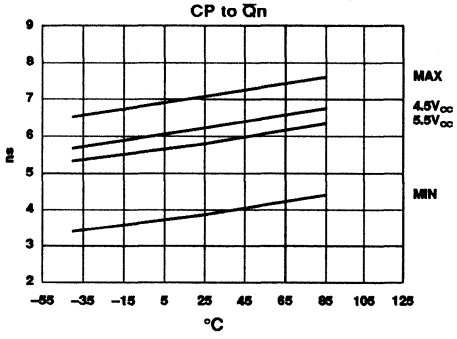
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
CP to $\overline{Q}$n



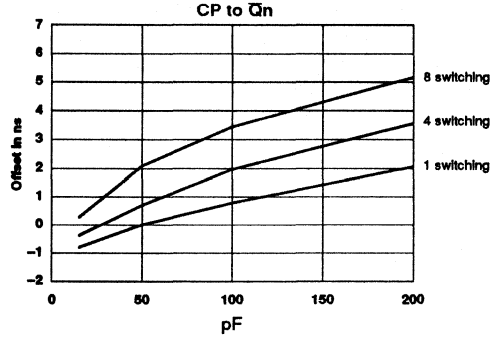
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
CP to $\overline{Q}$n



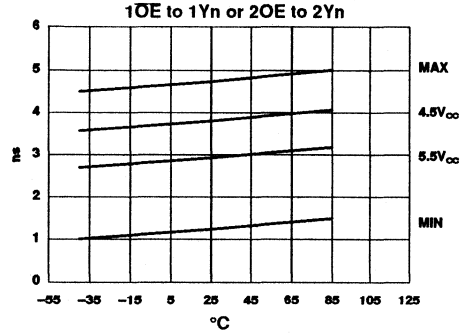
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
CP to $\overline{Q}$n



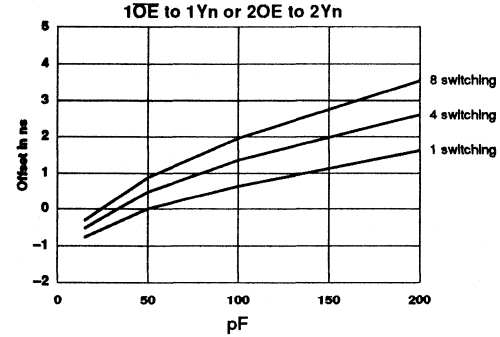
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
CP to $\overline{Q}$n



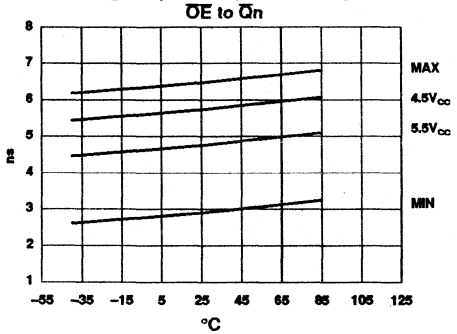
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
1$\overline{OE}$ to 1Yn or 2OE to 2Yn



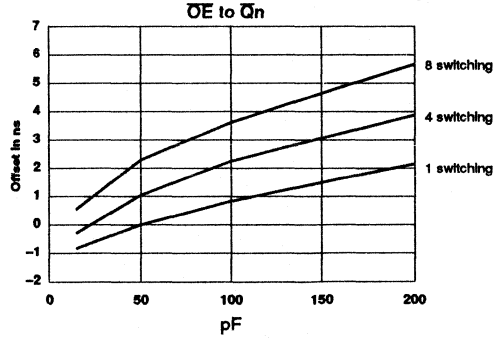
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
1$\overline{OE}$ to 1Yn or 2OE to 2Yn



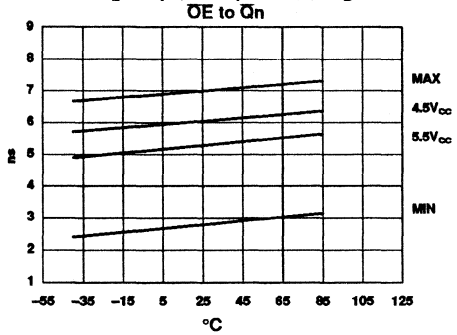
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to $\overline{Qn}$



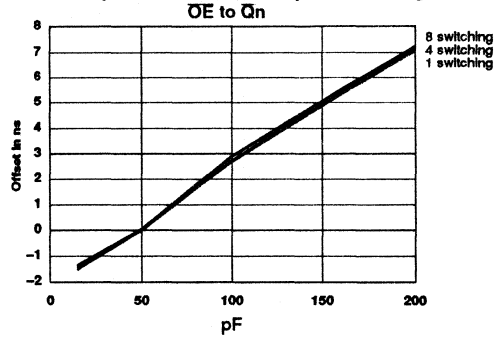
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to $\overline{Qn}$



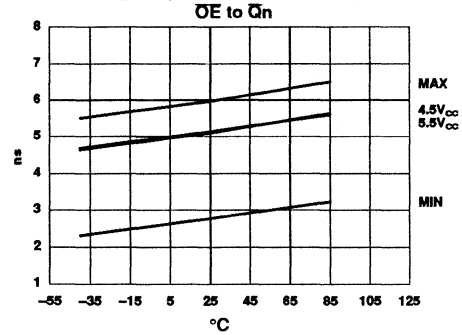
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to $\overline{Qn}$



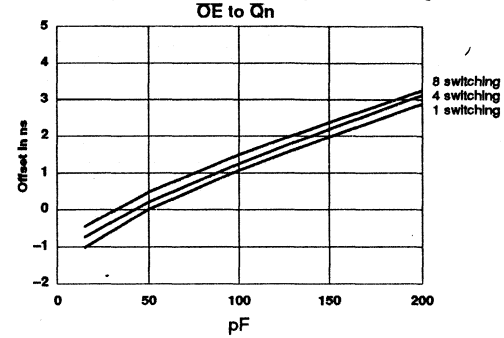
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to $\overline{Qn}$



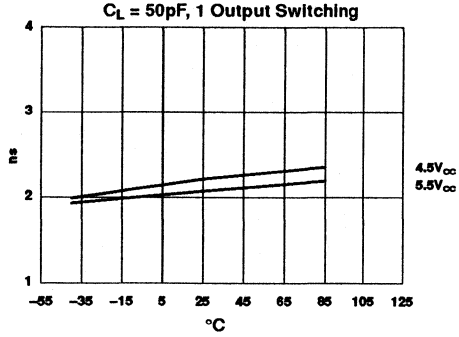
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to $\overline{Qn}$



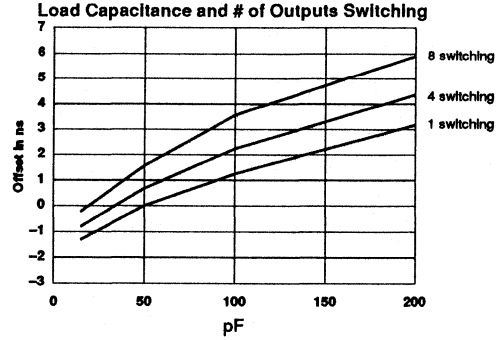
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to $\overline{Qn}$



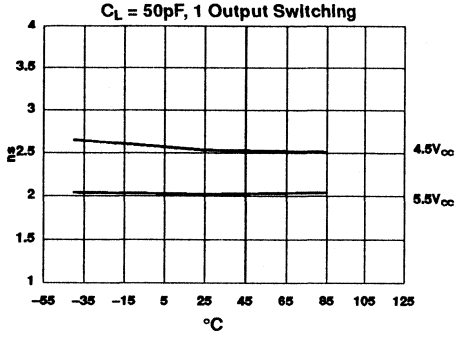
t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



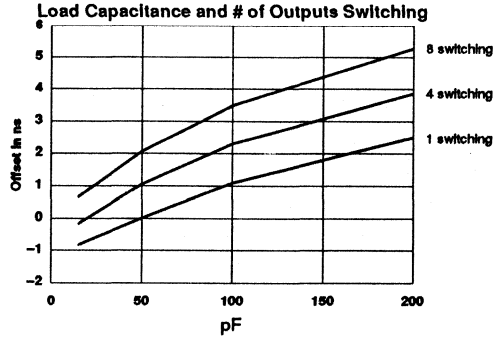
Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching



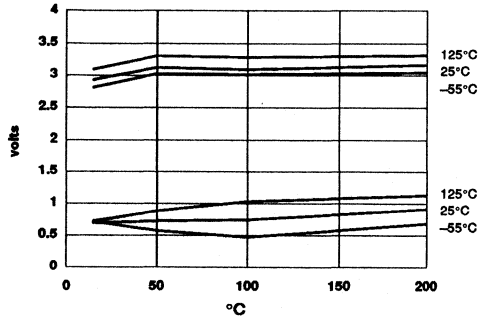
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



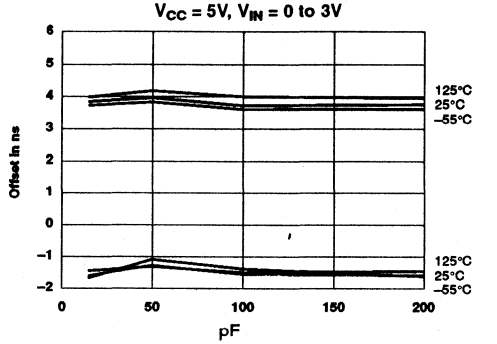
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching



V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



Octal buffer, inverting (3-State) — 74ABT540

FEATURES

- Octal bus interface
- 3-State buffers
- Efficient pinout to facilitate PC board layout
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT540 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT540 device is an inverting octal buffer that is ideal for driving bus lines. The device features input and outputs on opposite sides of the package to facilitate printed circuit board layout.

FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{OE0}$	$\overline{OE1}$	In	$\overline{Yn}$
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

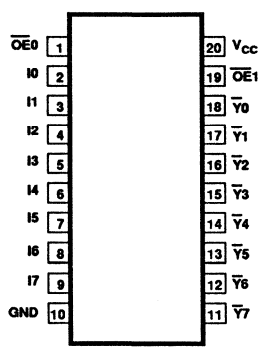
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT540N
20-pin plastic SOL	-40°C to +85°C	74ABT540D

PIN DESCRIPTION

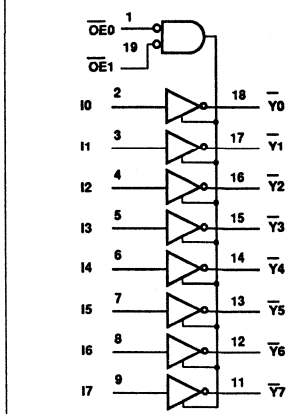
PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5 6, 7, 8, 9	In	Data inputs
18, 17, 16, 15 14, 13, 12, 11	$\overline{Yn}$	Data outputs
1, 19	$\overline{OE0}$, $\overline{OE1}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

PIN CONFIGURATION

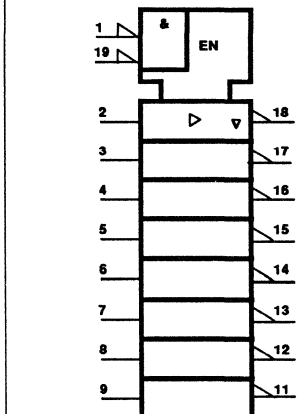


Top view

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Octal buffer/line driver (3-State)

74ABT541

FEATURES

- Octal bus interface
- Functions similar to the 'ABT241
- Provides ideal interface and increases fan-out of MOS Microprocessors
- Efficient pinout to facilitate PC board layout
- 3-State buffer outputs sink 64mA and source 32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT541 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT541 is an octal buffer that is ideal for driving bus lines. The outputs are all capable of sinking 64mA and sourcing 32mA. The device features inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay In to Yn	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

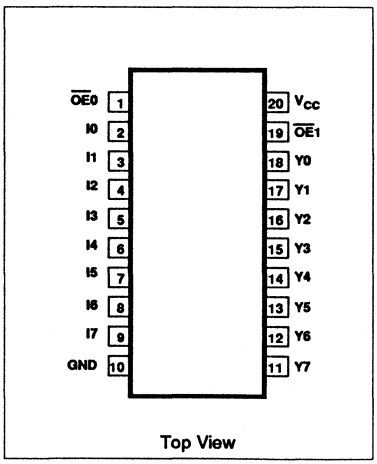
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT541N
20-pin plastic SOL	-40°C to +85°C	74ABT541D

PIN DESCRIPTION

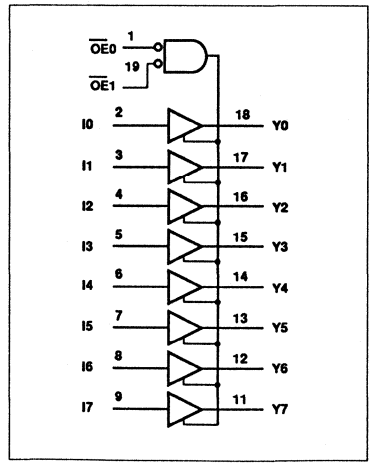
PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5 6, 7, 8, 9	In	Data inputs
18, 17, 16, 15 14, 13, 12, 11	Yn	Data outputs
1, 19	$\overline{OE}0$, $\overline{OE}1$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

PIN CONFIGURATION

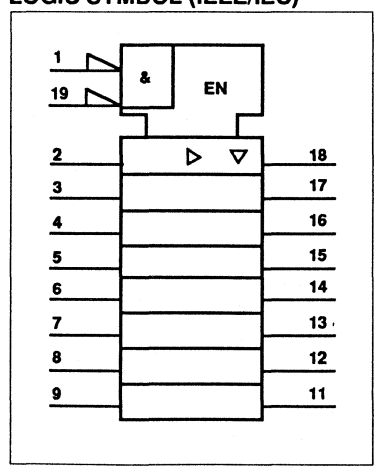


Top View

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE0}$	$\overline{OE1}$	In	Yn
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
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3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

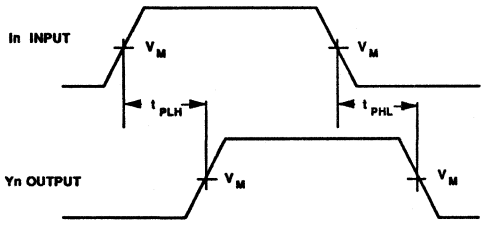
AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

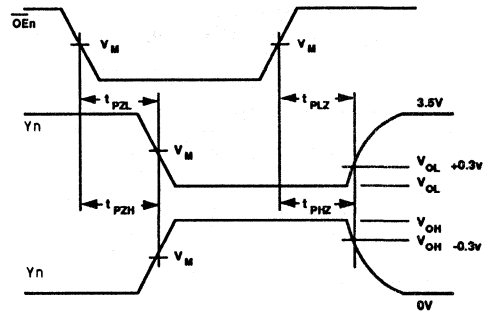
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40° C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Yn	1	1.0 1.0	2.6 2.9	4.1 4.2	1.0 1.0	4.6 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 2.1	3.1 4.4	4.8 5.9	1.1 2.1	5.3 6.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.1 1.7	5.1 4.7	6.6 6.2	2.1 1.7	7.1 6.7	ns

AC WAVEFORMS

(V_M = 1.5V, V_{IN} = GND to 3.0V)

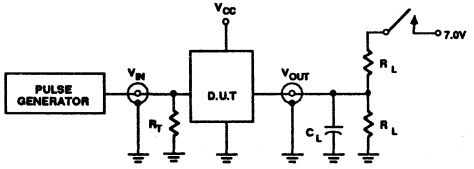


Waveform 1. Waveforms Showing the Input (In) to Output (Yn) Propagation Delays

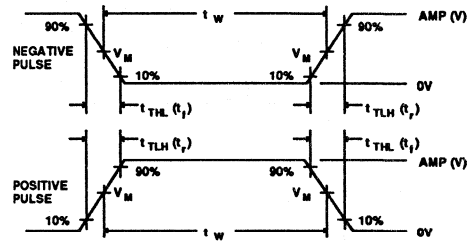


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

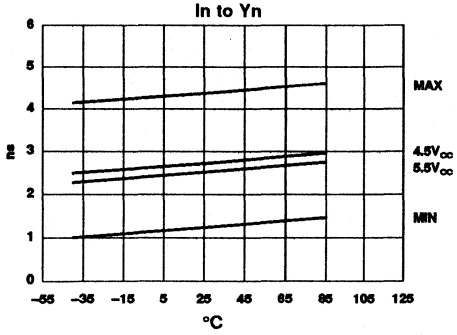
R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

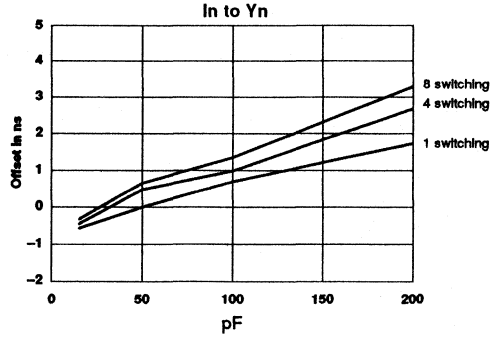
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

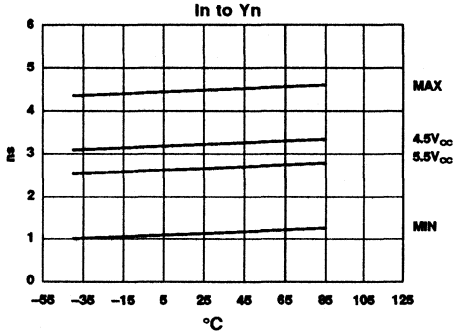
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
In to Yn



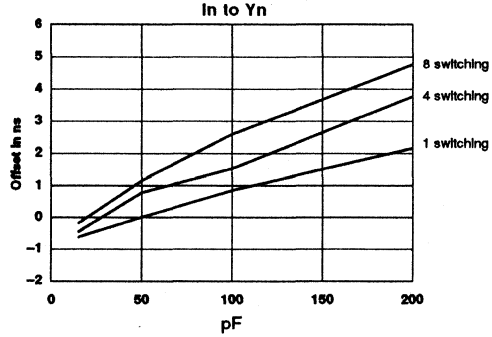
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
In to Yn



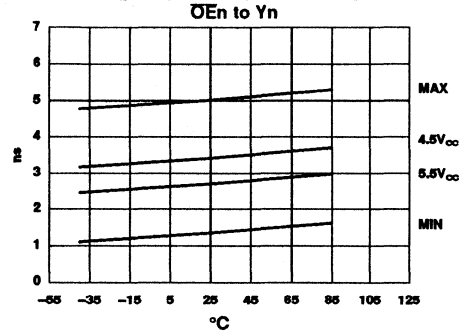
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
In to Yn



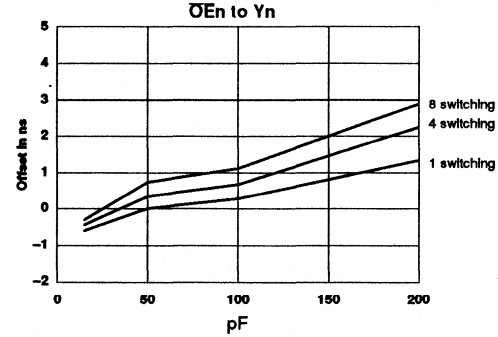
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
In to Yn



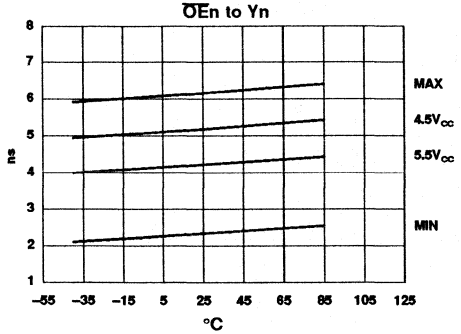
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$n to Yn



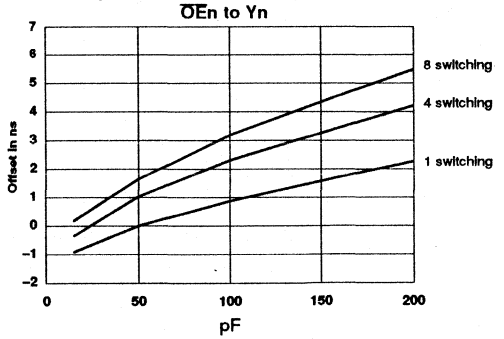
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$n to Yn



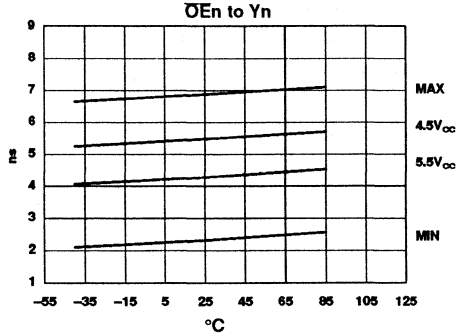
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$n to Yn



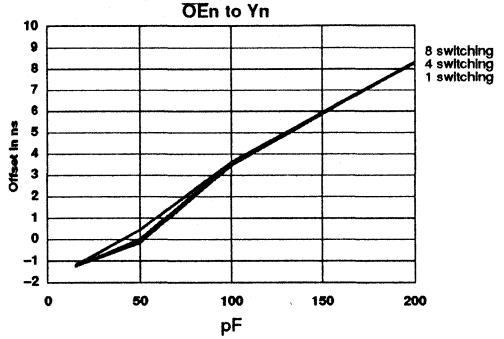
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$n to Yn



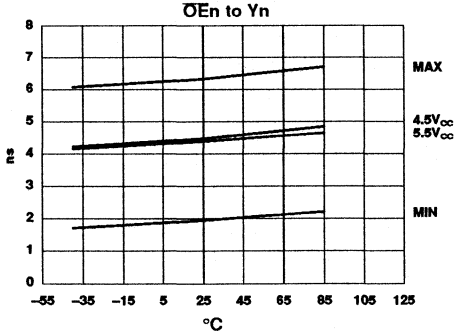
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$n to Yn



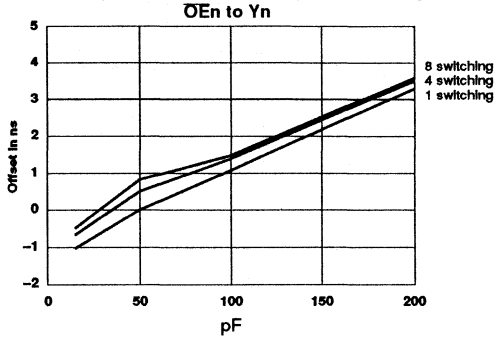
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$n to Yn



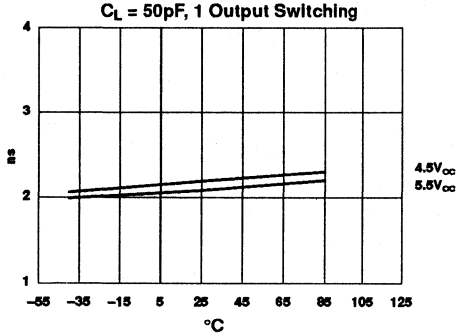
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$n to Yn



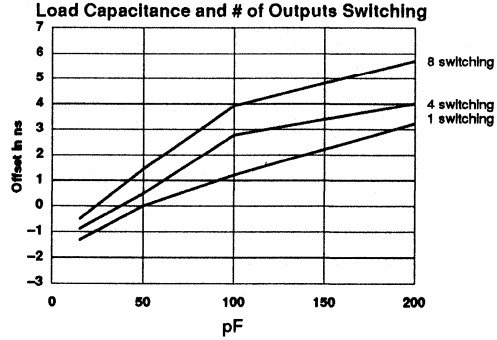
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$n to Yn



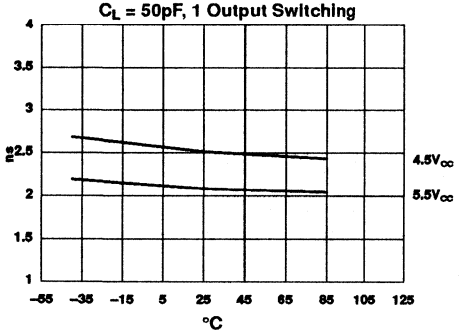
t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



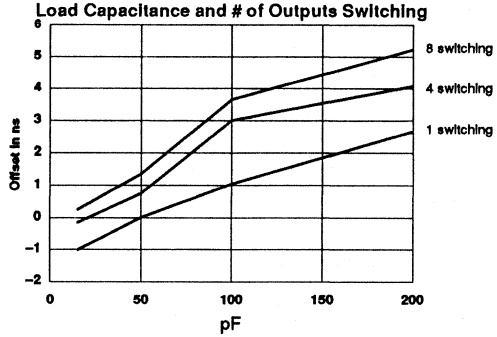
Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching



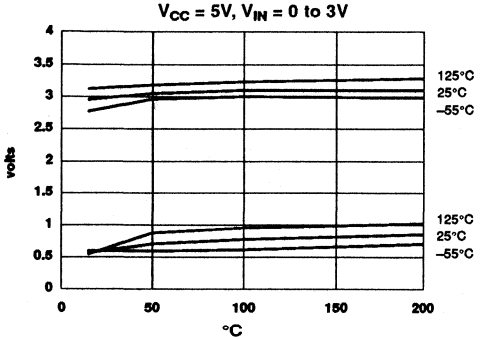
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



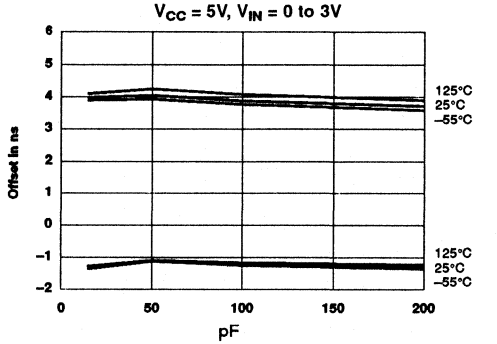
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching



V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



Octal latched transceiver with dual enable (3-State)

74ABT543

FEATURES

- Combines 74ABT245 and 74ABT373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT543 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT543 Octal Registered Transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64mA.

FUNCTIONAL DESCRIPTION

The 'ABT543 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($\overline{EAB}$) input and the A-to-B Latch Enable ($\overline{LEAB}$) input are Low the A-to-B path is transparent. A subsequent Low-to High transition of the $\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A in-

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn	C_L = 50pF; V_{CC} = 5V	4.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

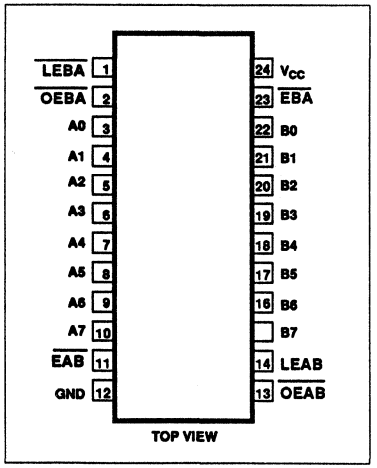
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT543N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT543D

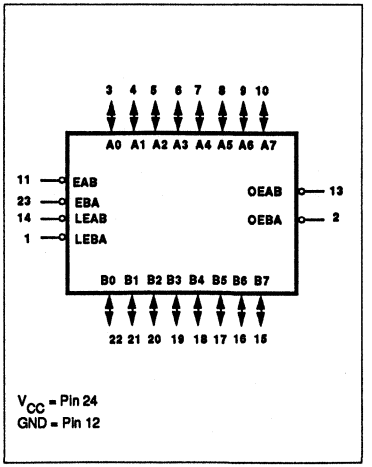
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
14, 1	$\overline{LEAB}$ / $\overline{LEBA}$	A to B / B to A Latch Enable input (Active Low)
11, 23	$\overline{EAB}$ / $\overline{EBA}$	A to B / B to A Enable input (Active Low)
13, 2	$\overline{OEAB}$ / $\overline{OEBA}$	A to B / B to A Output Enable input (Active Low)
3, 4, 5, 6 7, 8, 9, 10	A0 - A7	Port A, 3-State outputs
22, 21, 20, 19 18, 17, 16, 15	B0 - B7	Port B, 3-State outputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

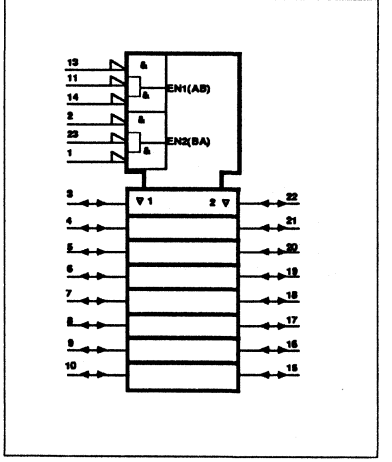
PIN CONFIGURATION



LOGIC SYMBOL

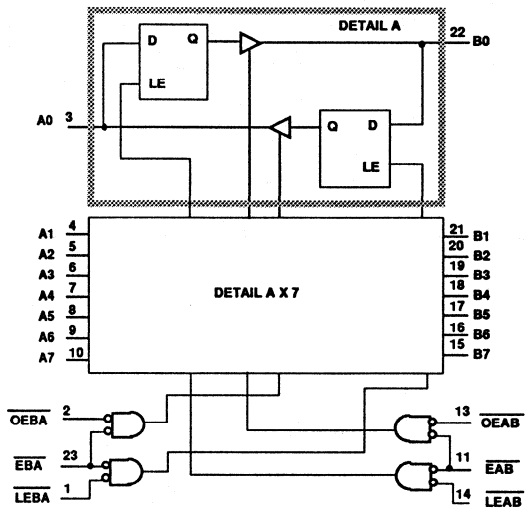


LOGIC SYMBOL(IEEE/IEC)



Octal latched transceiver with dual enable (3-State) 74ABT543

LOGIC DIAGRAM



V_{CC}=Pin 24
GND=Pin 12

puts. With $\overline{EAB}$ and $\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

FUNCTION TABLE

INPUTS $\overline{OEXX}$	INPUTS $\overline{EXX}$	INPUTS $\overline{LEXX}$	INPUTS DATA	OUTPUTS	STATUS
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L	↑	L	h	Z	Disabled + Latch
L	↑	L	l	Z	
L	L	↑	h	H	Latch + Display
L	L	↑	l	L	
L	L	L	H	H	Transparent
L	L	L	L	L	
L	L	H	X	NC	Hold

H= High voltage level
L= Low voltage level
h= High state must be present one setup time before the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
l = Low state must be present one setup time before the Low-to -High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
↑ =Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
X=Don't care
NC=No change
Z =High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
I_{IH} + I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC ELECTRICAL CHARACTERISTICS

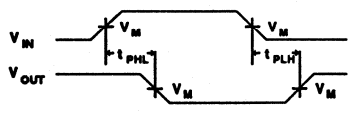
GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V			T_{amb} = -40°C to +85°C, V_{CC} = 5V±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	Waveform 2	1.9 1.9	4.4 4.4	5.9 5.9	1.9 1.9	6.9 6.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn	Waveform 1, 2	1.6 2.1	4.1 4.6	5.6 6.1	1.6 2.1	6.6 7.1	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	Waveform 4 Waveform 5	1.4 2.5	3.9 5.0	5.4 6.5	1.4 2.5	6.4 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	Waveform 4 Waveform 5	3.4 3.0	5.9 5.5	7.4 7.0	3.4 3.0	8.4 8.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{EBA}$ to An, $\overline{EAB}$ to Bn	Waveform 4 Waveform 5	1.4 2.5	3.9 5.0	5.4 6.5	1.4 2.5	6.4 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{EBA}$ to An, $\overline{EAB}$ to Bn	Waveform 4 Waveform 5	3.4 3.0	5.9 5.5	7.4 7.0	3.4 3.0	8.4 8.0	ns

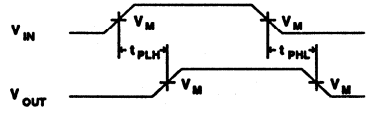
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V			T_{amb} = -40°C to +85°C, V_{CC} = 5V±0.5V		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	Waveform 3	3.5 3.0			3.5 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	Waveform 3	0.5 0.5			0.5 0.5		ns
$t_s(H)$ $t_s(L)$	Setup time An to $\overline{EAB}$, Bn to $\overline{EBA}$	Waveform 3	3.5 3.0			3.5 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time An to $\overline{EAB}$, Bn to $\overline{EBA}$	Waveform 3	0.5 0.5			0.5 0.5		ns
$t_w(L)$	Latch enable pulse width, Low	Waveform 3	3.5			3.5		ns

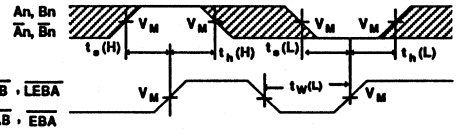
AC WAVEFORMS



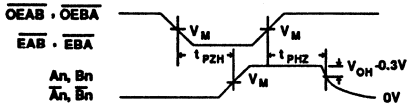
Waveform 1. Propagation Delay For Inverting Output



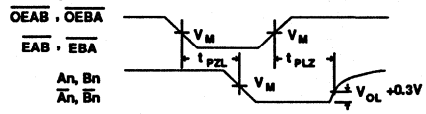
Waveform 2. Propagation Delay For Non-Inverting Output



Waveform 3. Data Setup And Hold Times And Latch Enable pulse width



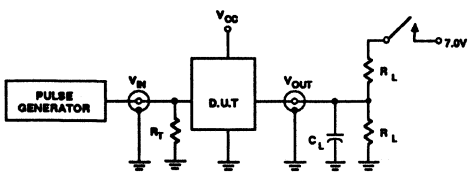
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output

TEST CIRCUIT AND WAVEFORMS



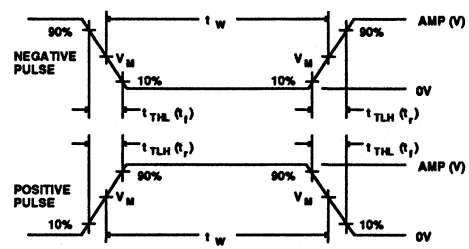
Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

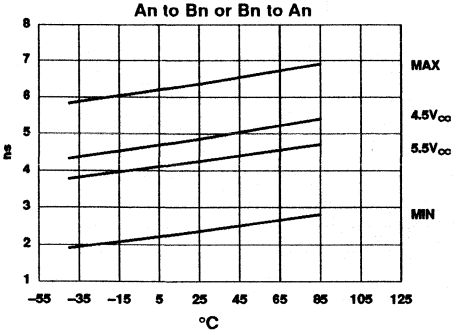
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



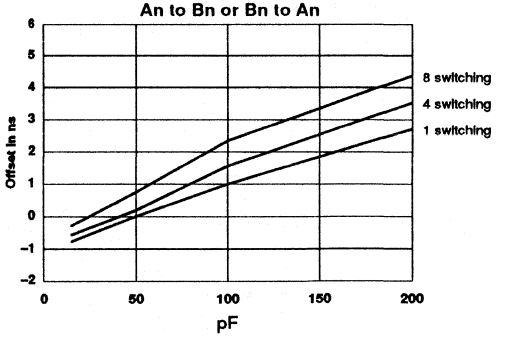
V_M = 1.5V
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

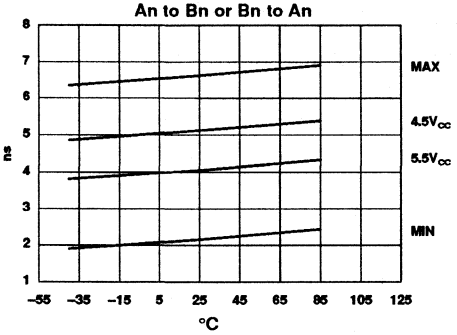
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
An to Bn or Bn to An



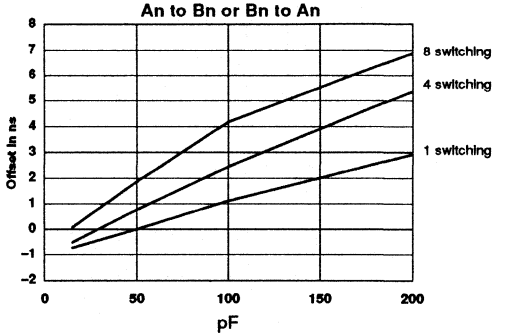
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
An to Bn or Bn to An



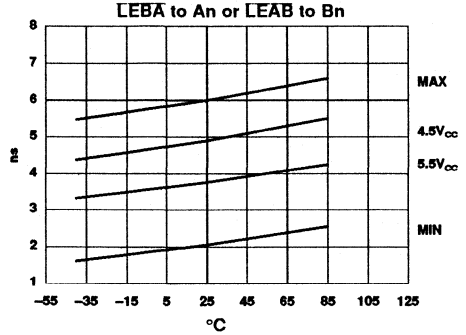
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
An to Bn or Bn to An



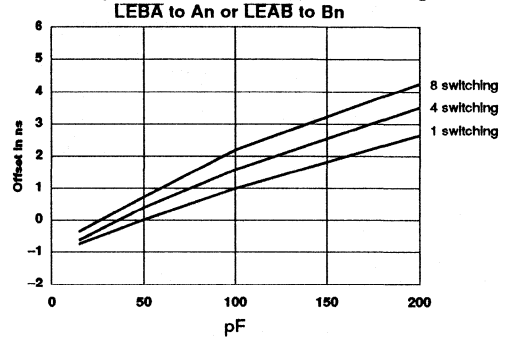
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
An to Bn or Bn to An



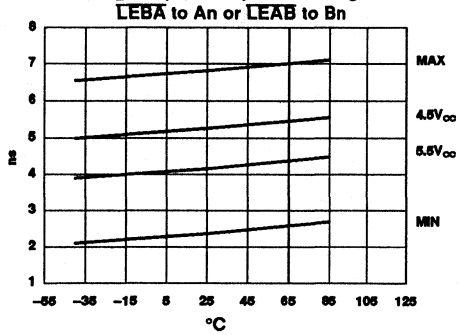
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{LEBA}$ to An or $\overline{LEAB}$ to Bn



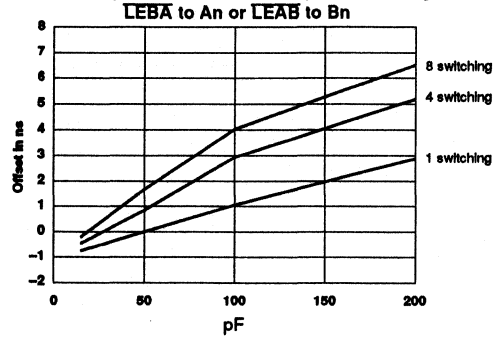
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
$\overline{LEBA}$ to An or $\overline{LEAB}$ to Bn



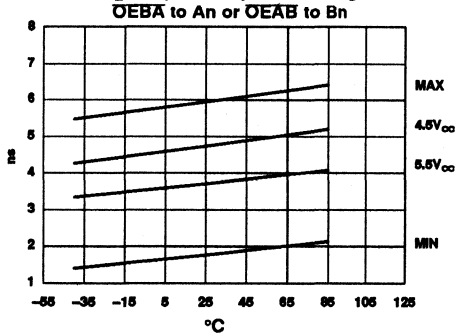
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{LEBA}$ to An or $\overline{LEAB}$ to Bn



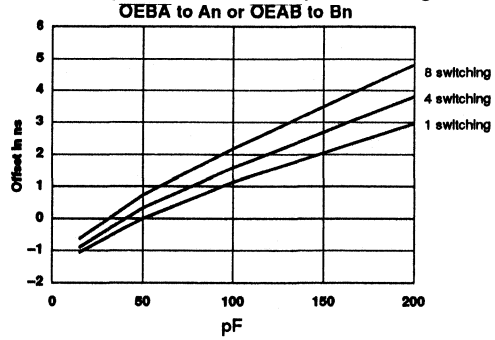
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
$\overline{LEBA}$ to An or $\overline{LEAB}$ to Bn



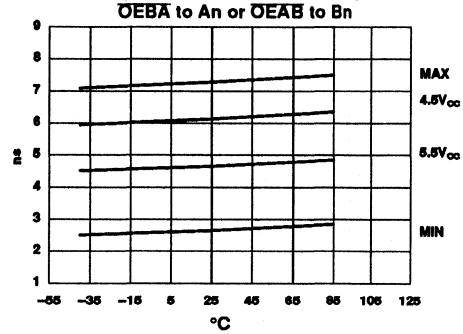
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



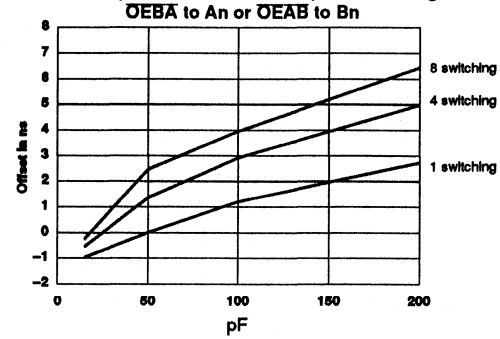
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



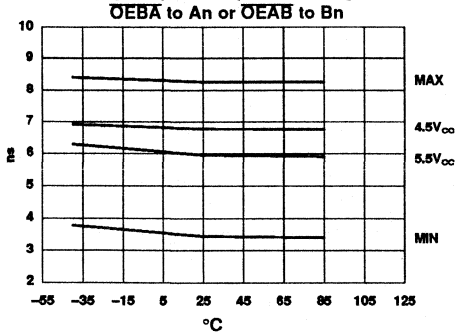
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



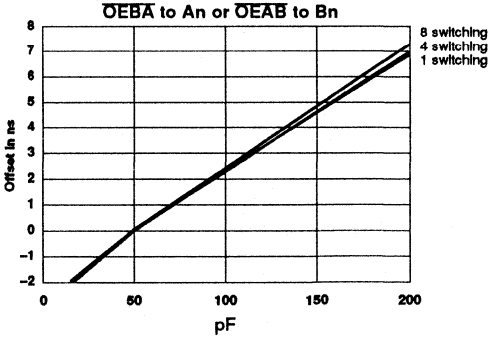
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



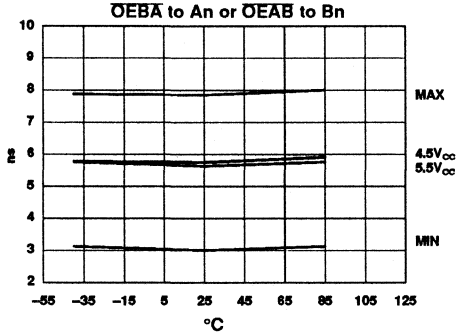
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



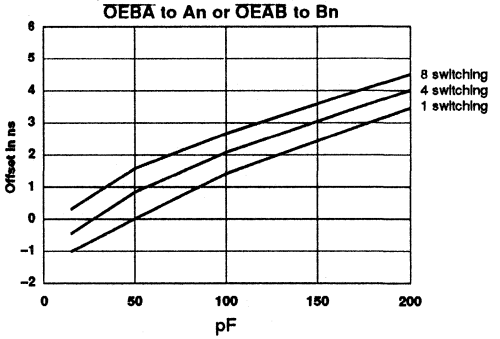
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



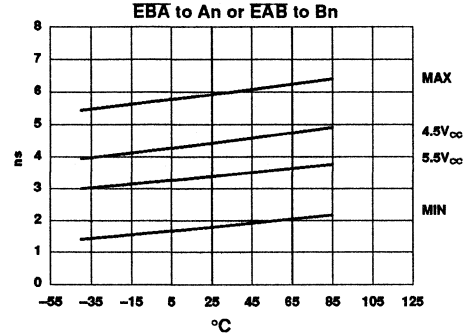
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



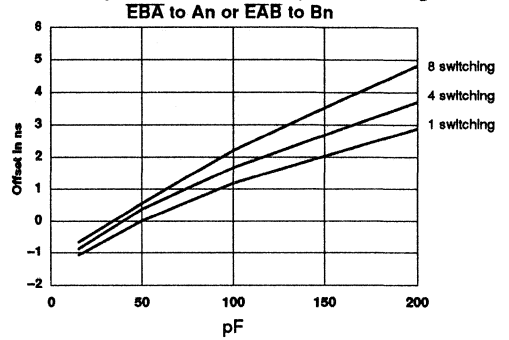
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



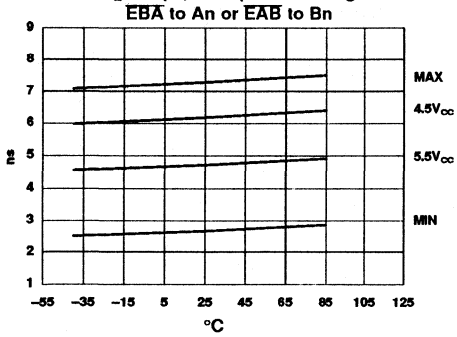
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{EBA}$ to An or $\overline{EAB}$ to Bn



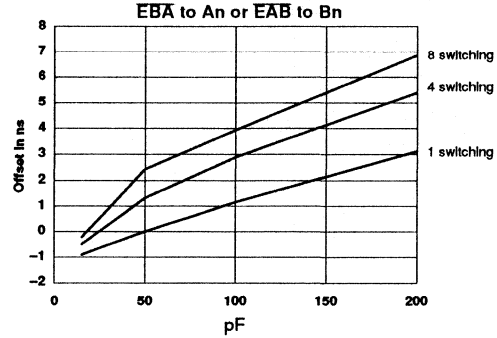
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$\overline{EBA}$ to An or $\overline{EAB}$ to Bn



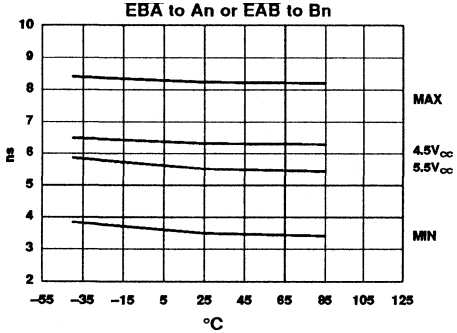
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{EBA}$ to An or $\overline{EAB}$ to Bn



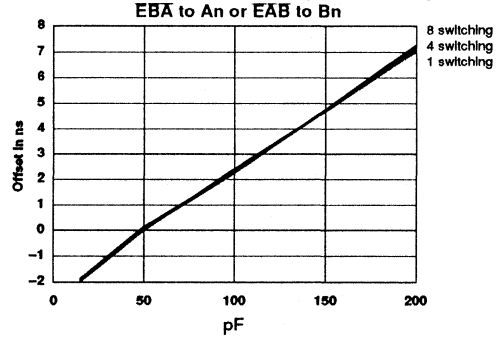
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$\overline{EBA}$ to An or $\overline{EAB}$ to Bn



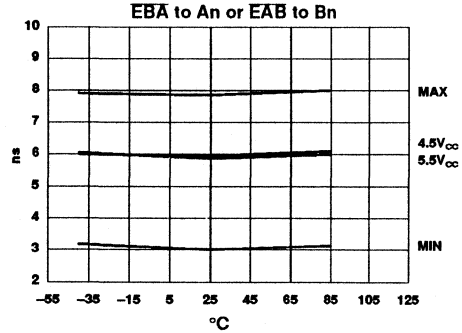
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{EBA}$ to An or $\overline{EAB}$ to Bn



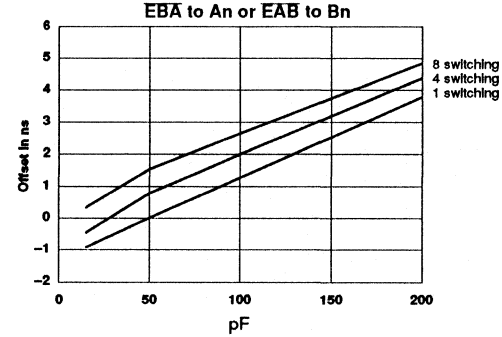
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$\overline{EBA}$ to An or $\overline{EAB}$ to Bn



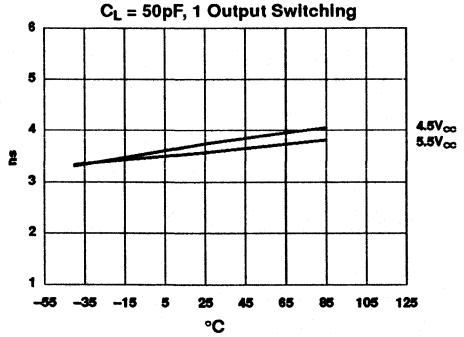
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{EBA}$ to An or $\overline{EAB}$ to Bn



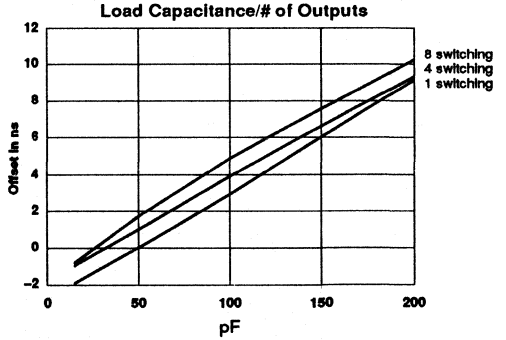
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$\overline{EBA}$ to An or $\overline{EAB}$ to Bn



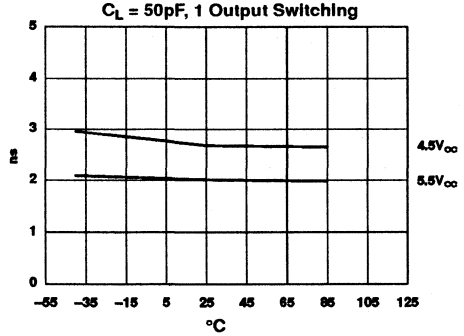
t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



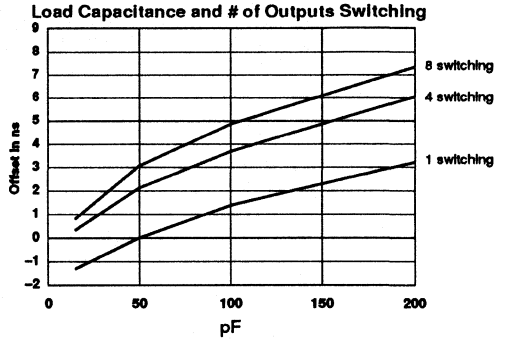
Adjustment of t_{TLH} for
Load Capacitance/# of Outputs



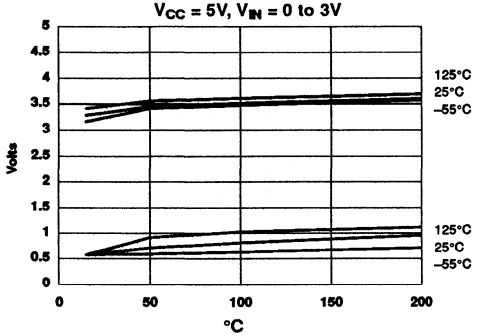
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



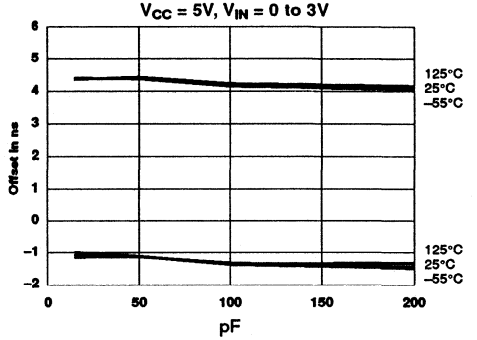
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching



V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



Octal latched transceiver with dual enable, inverting — 74ABT544

FEATURES

- Combines 74ABT245 and 74ABT373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 3-State buffer outputs sink 64mA and source 32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT544 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT544 Octal Registered Transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The outputs are guaranteed to sink 64mA.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Anto Bn	C_L = 50pF; V_{CC} = 5V	4.3	ns
C_{IN}	Input capacitance $\overline{LE}$, $\overline{E}$, $\overline{OE}$	V_I = 0V or V_{CC}	4	pF
C_{OUT}	I/O capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

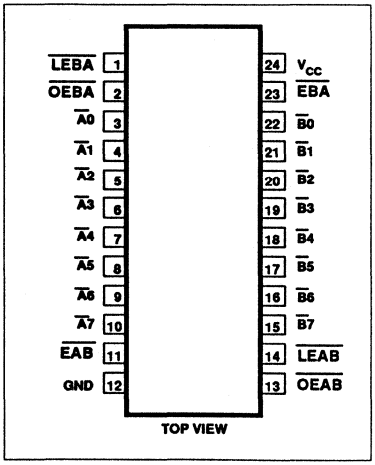
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT544N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT544D

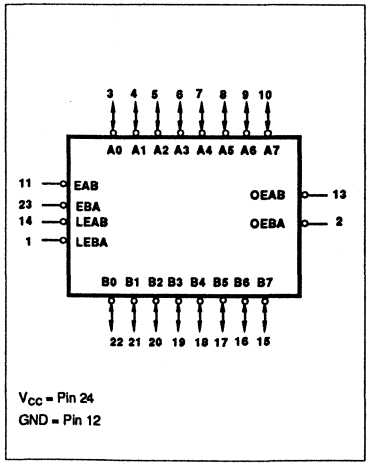
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
14, 1	$\overline{LEAB}$ / $\overline{LEBA}$	A to B / B to A Latch Enable input (Active Low)
11, 23	$\overline{EAB}$ / $\overline{EBA}$	A to B / B to A Enable input (Active Low)
13, 2	$\overline{OEAB}$ / $\overline{OEBA}$	A to B / B to A Output Enable input (Active Low)
3, 4, 5, 6 7, 8, 9, 10	$\overline{A0}$ - $\overline{A7}$	Port $\overline{A}$, 3-State outputs
22, 21, 20, 19 18, 17, 16, 15	$\overline{B0}$ - $\overline{B7}$	Port $\overline{B}$, 3-State outputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

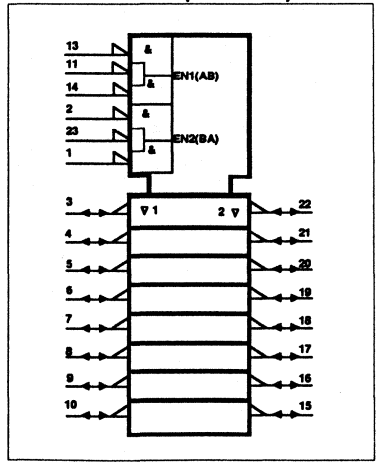
PIN CONFIGURATION



LOGIC SYMBOL

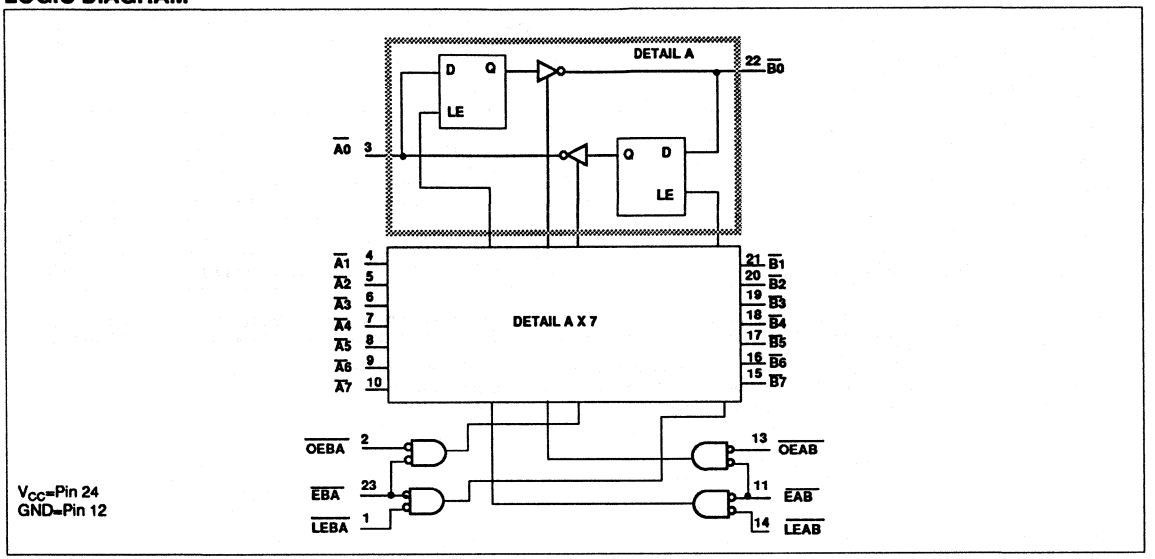


LOGIC SYMBOL(IEEE/IEC)



Octal latched transceiver with dual enable, inverting | 74ABT544

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The 'ABT544 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($\overline{EAB}$) input and the A-to-B Latch Enable ($\overline{LEAB}$) input are Low the A-to-B path is transparent. A subsequent Low-to High transition of the $\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both Low, the 3-State B output buffers are active and invert the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
OEXX	$\overline{EXX}$	LEXX	DATA		
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	L H	Latch + Display
L L	L L	L L	H L	L H	Transparent
L	L	H	X	NC	Hold

H= High voltage level
L= Low voltage level
h= High state must be present one setup time before the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
l = Low state must be present one setup time before the Low-to -High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
↑ =Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
X=Don't care
NC=No change
Z =High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
I_{IH} + I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Octal D-type transparent latch (3-State) 74ABT573

DESCRIPTION

- 74ABT573 is broadside pinout version of 74ABT373
- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-State Outputs for bus interfacing
- Common output enable
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT573 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT573 device is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates. The 74ABT573 is functionally identical to the 74ABT373 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50pF; V_{CC} = 5V	4.2	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

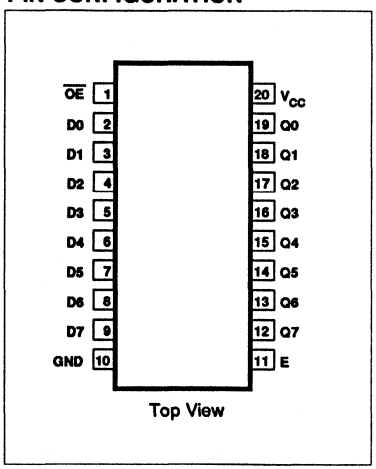
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT573N
20-pin plastic SOL	-40°C to +85°C	74ABT573D

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

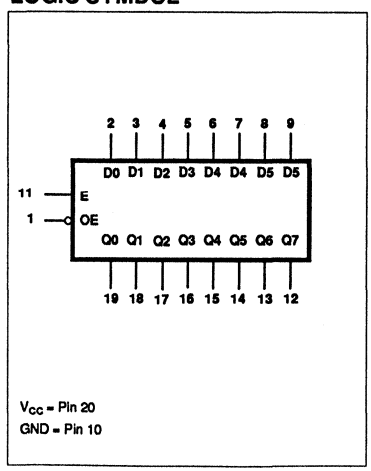
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

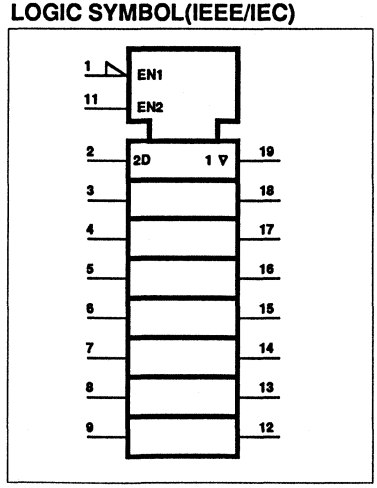
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Octal D-type transparent latch (3-State) 74ABT573

PIN DESCRIPTION

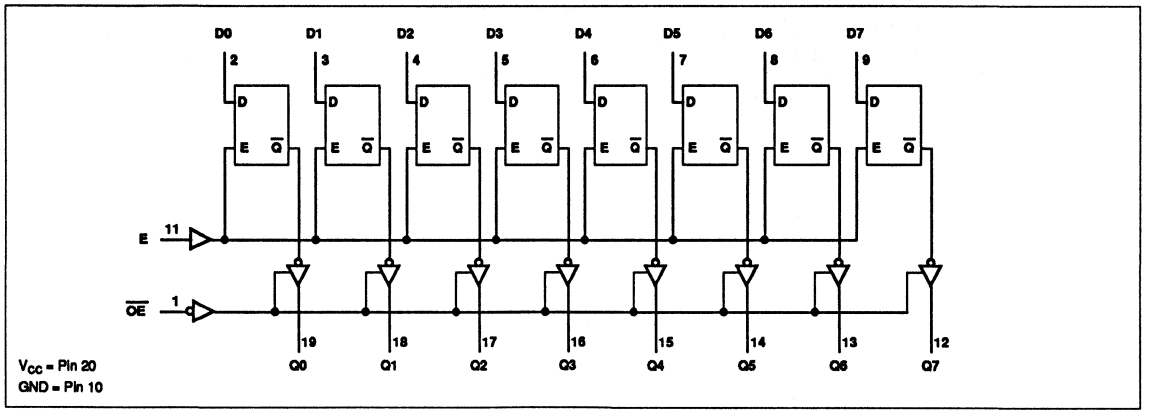
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output enable input (active Low)
2, 3, 4, 5 6, 7, 8, 9	D0 - D7	Data inputs
19, 18, 17, 16 15, 14, 13, 12	Q0 - Q7	3-State Outputs
11	E	Enable input (active High)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	Dn	REGISTER	Q0 - Q7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	Waveform 2	1.9 2.2	3.2 4.2	5.4 5.7	1.9 2.2	5.9 6.2	ns
t_{PLH} t_{PHL}	Propagation delay E to Qn	Waveform 1	2.2 3.2	4.0 5.2	6.1 6.7	2.2 3.2	6.6 7.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	Waveform 4 Waveform 5	1.2 2.7	3.2 4.7	4.7 6.2	1.2 2.7	5.2 6.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	Waveform 4 Waveform 5	2.5 2.0	4.9 4.2	6.4 6.0	2.5 2.0	6.9 6.5	ns

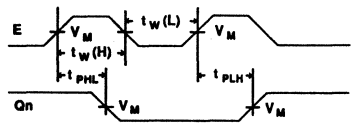
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

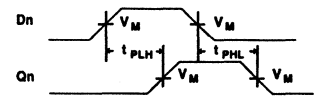
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Set-up time Dn to E	Waveform 3	1.9 1.5			1.9 1.5		ns
t_h(H) t_h(L)	Hold time Dn to E	Waveform 3	1.0 1.0			1.0 1.0		ns
t_W(H)	E pulse width, High or Low	Waveform 1	3.3			3.3		ns

AC WAVEFORMS

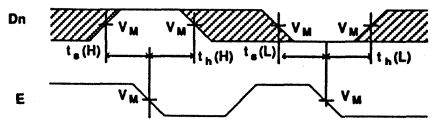
(V_M = 1.5V, V_{IN} = GND to 3.0V)



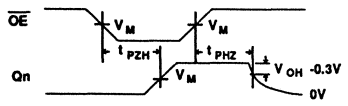
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width.



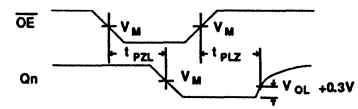
Waveform 2. Propagation Delay for Data to Outputs.



Waveform 3. Data Setup and Hold Times.

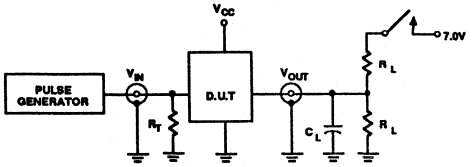


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time From High Level.



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

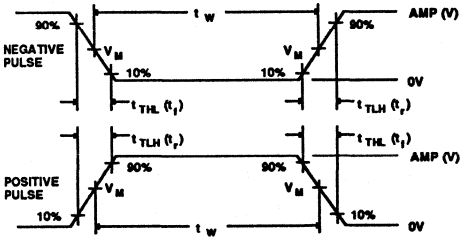
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

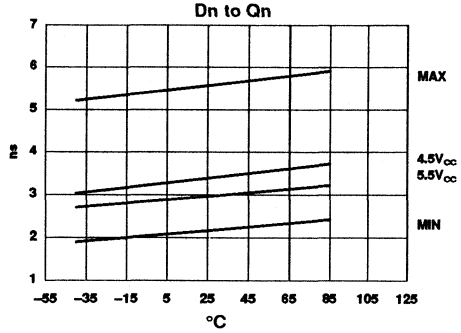


V_M = 1.5V

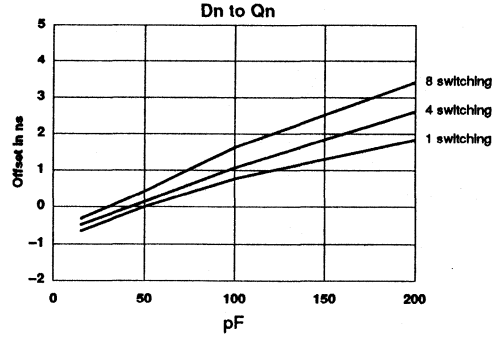
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

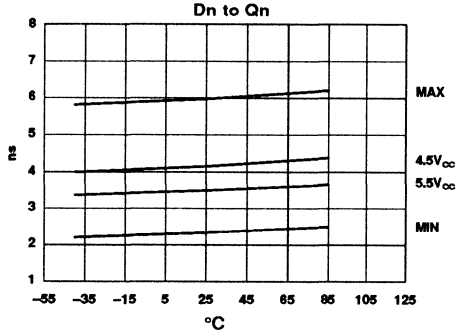
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
Dn to Qn



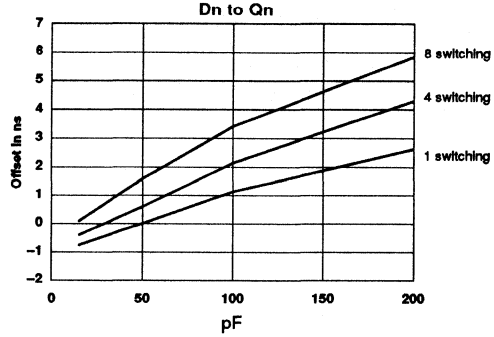
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
Dn to Qn



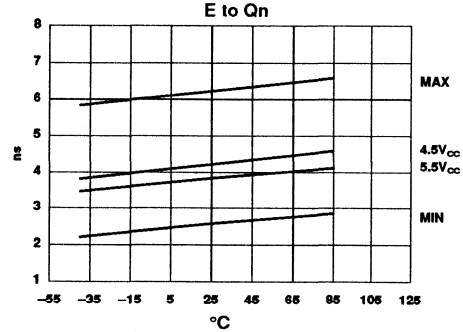
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
Dn to Qn



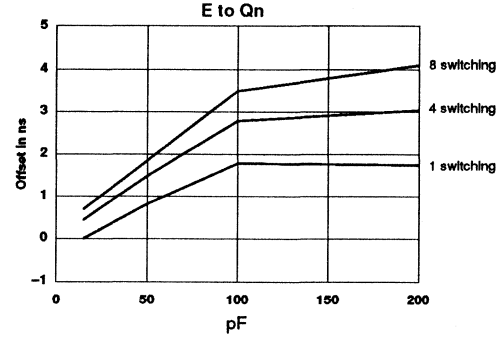
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
Dn to Qn



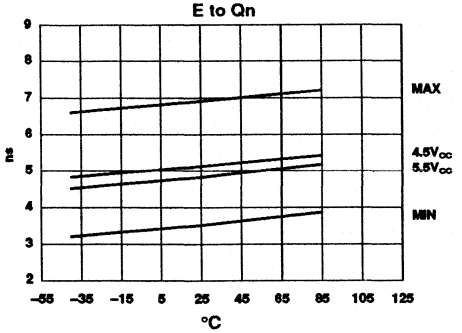
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
E to Qn



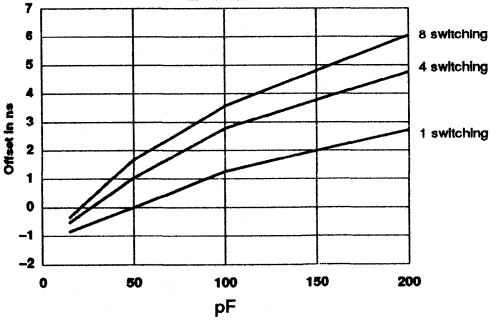
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
E to Qn



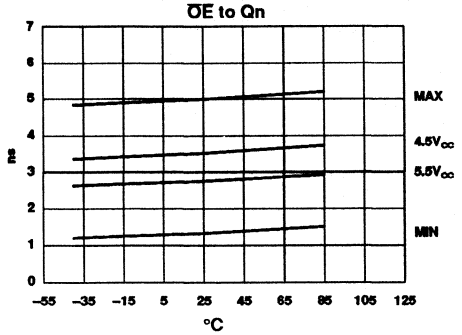
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
E to Qn



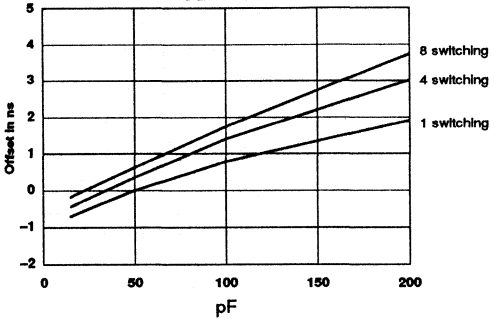
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
E to Qn



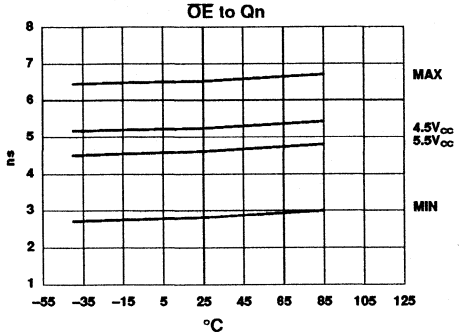
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to Qn



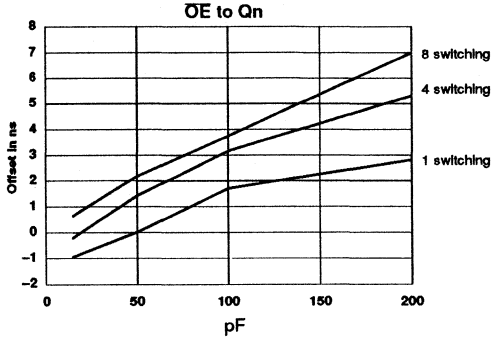
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to Qn



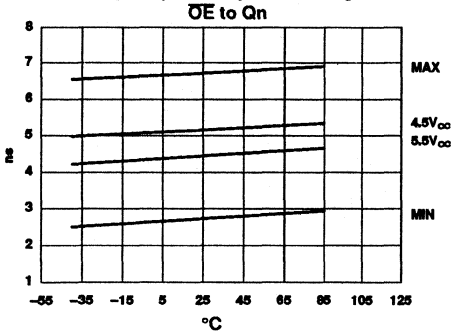
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to Qn



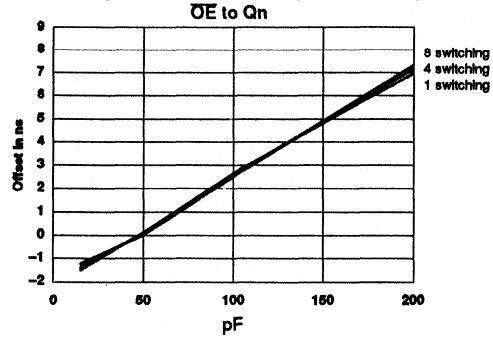
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to Qn



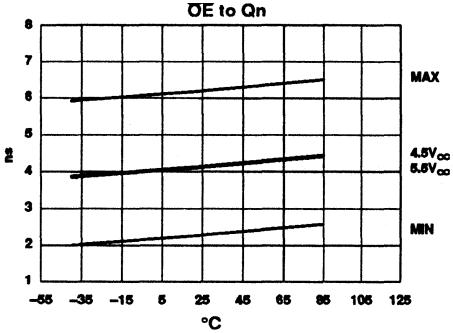
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to Qn



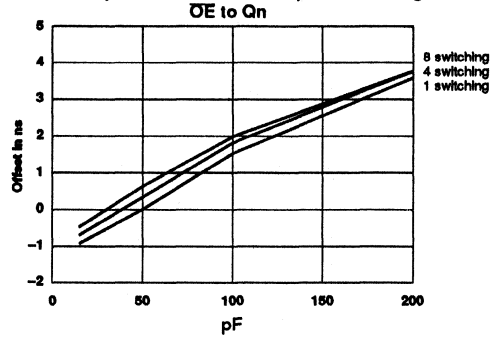
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to Qn



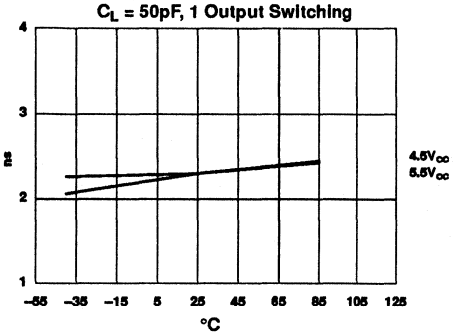
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to Qn



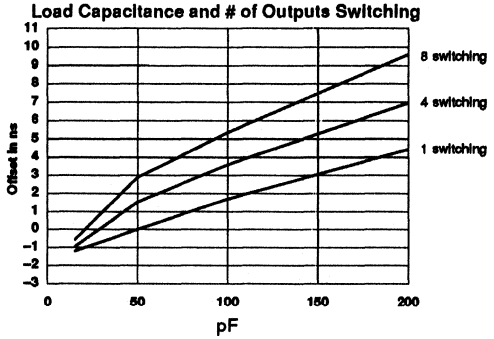
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to Qn

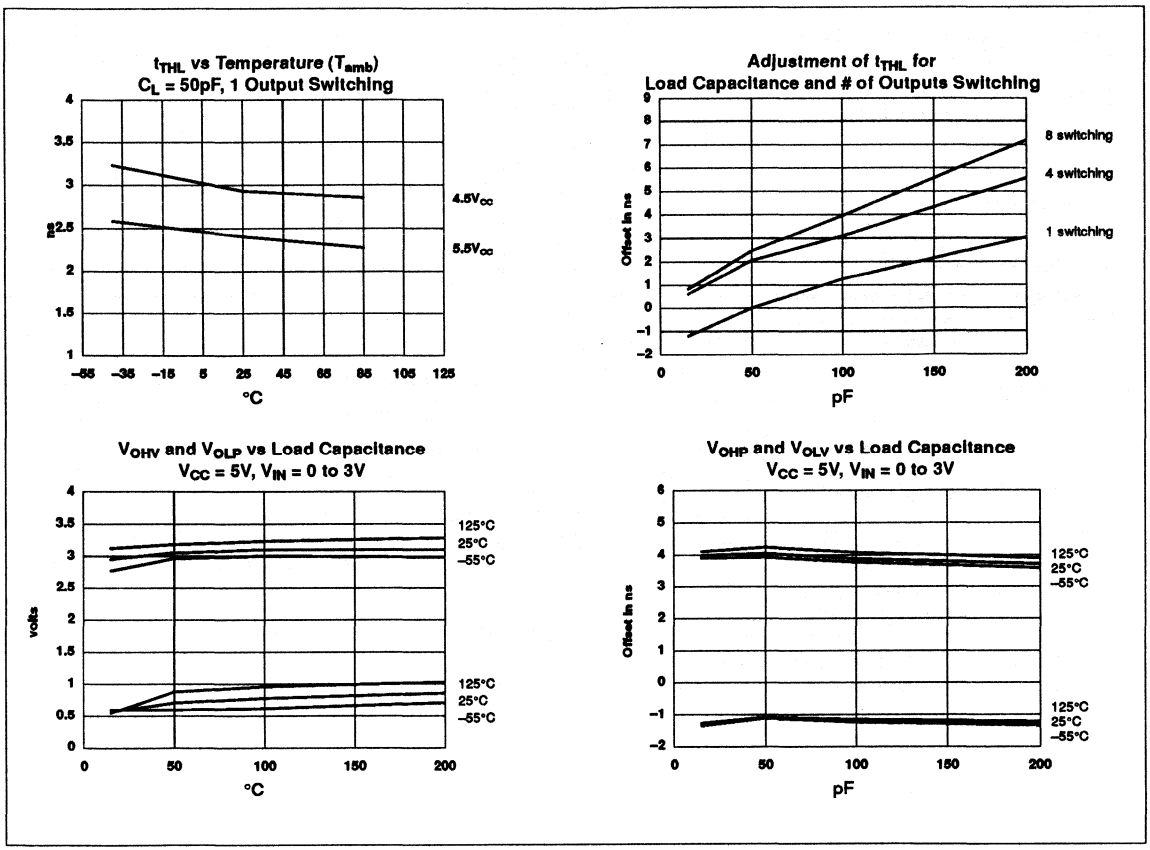


t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching




t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
4.5V$_{CC}$
5.5V$_{CC}$
°C
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching
Offset in ns
8 switching
4 switching
1 switching
pF
V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
volts
125°C
25°C
–55°C
°C
V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
Offset in ns
pF

Octal D-type flip-flop (3-State) 74ABT574

FEATURES

- 74ABT574 is broadside pinout version of 74ABT374
- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-State outputs for bus interfacing
- Common output enable
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT574 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT574 device is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by clock (CP) and Output Enable ($\overline{OE}$) control gates. The state of each D input (one set-up time before the Low-to-High clock transition) is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the clock operation. When $\overline{OE}$ is Low, the data appears at the outputs. When $\overline{OE}$ is High, the outputs are in a high impedance "off" state, which means they will neither drive nor load the bus.

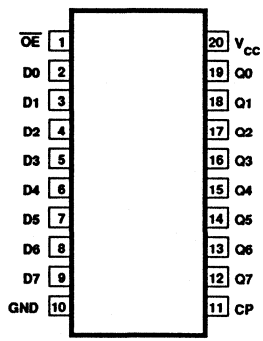
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	4.8	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

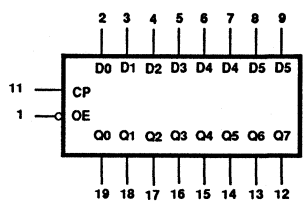
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT574N
20-pin plastic SOL	-40°C to +85°C	74ABT574D

PIN CONFIGURATION



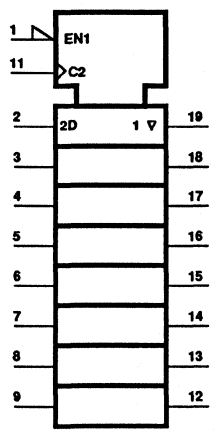
Top View

LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)



Octal D-type flip-flop (3-State) 74ABT574

PIN DESCRIPTION

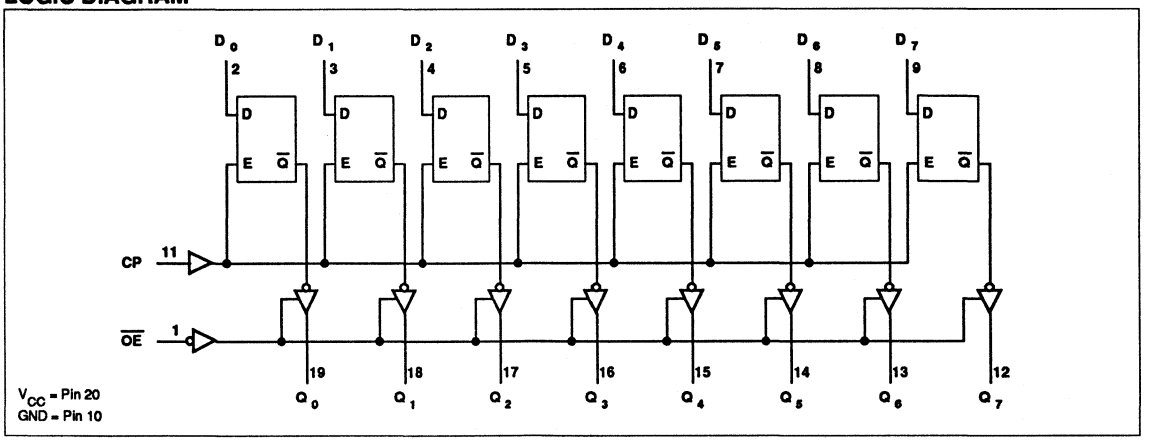
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output enable input (active Low)
2, 3, 4, 5 6, 7, 8, 9	D0 - D7	Data inputs
19, 18, 17, 16 15, 14, 13, 12	Q0 - Q7	3-State Outputs
11	CP	Clock Pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn	REGISTER	Q0 - Q7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	‡	X	NC	NC	Hold
H H	↑ X	Dn X	Dn X	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
‡ = Not a Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40° C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	150	200		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	Waveform 1	2.2 3.0	3.9 4.8	6.2 6.6	2.2 3.0	6.8 7.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	Waveform 3 Waveform 4	1.0 2.5	3.3 4.7	4.3 5.9	1.0 2.5	5.1 6.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	Waveform 3 Waveform 4	2.4 2.0	4.9 4.0	6.2 5.8	2.4 2.0	7.0 6.5	ns

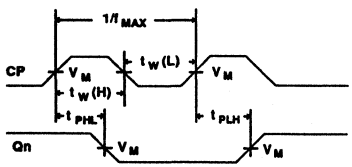
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

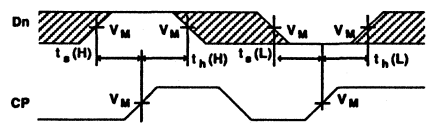
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40° C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time Dn to CP	Waveform 2	1.0 1.5			1.0 1.5		ns
$t_h(H)$ $t_h(L)$	Hold time Dn to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_W(H)$ $t_W(L)$	CP pulse width, High or Low	Waveform 1	3.3 3.3			3.3 3.3		ns

AC WAVEFORMS

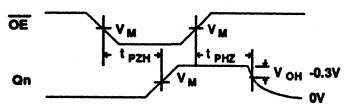
(V_M = 1.5V, V_{IN} = GND to 3.0V)



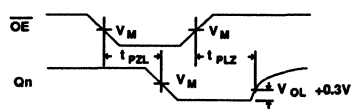
Waveform 1. Propagation Delay, Clock to Output, Clock Pulse Width and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times

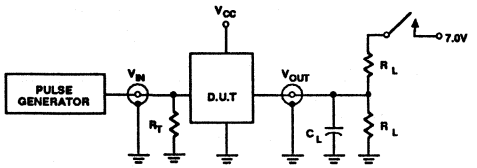


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

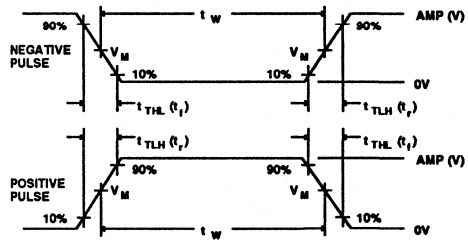
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

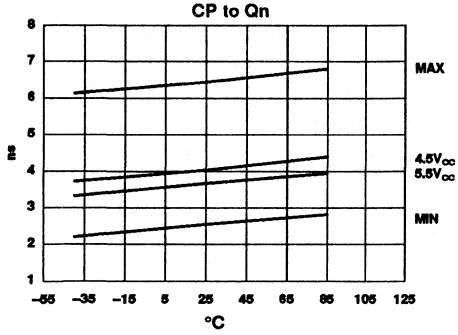


V_M = 1.5V

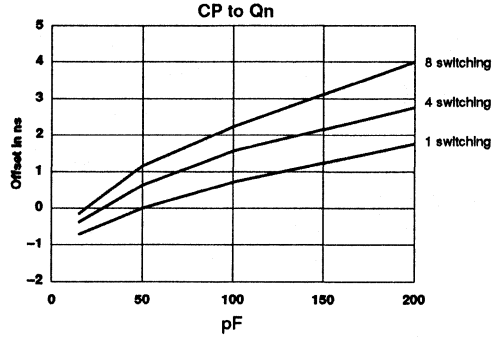
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

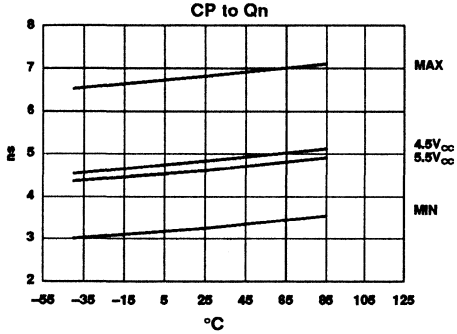
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
CP to Qn



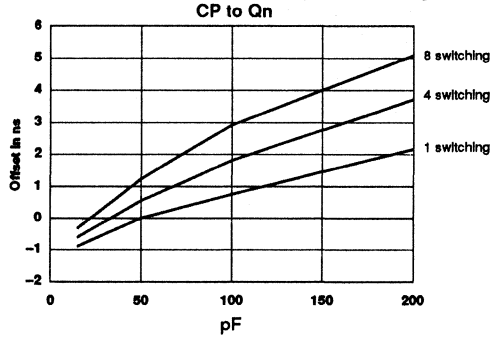
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
CP to Qn



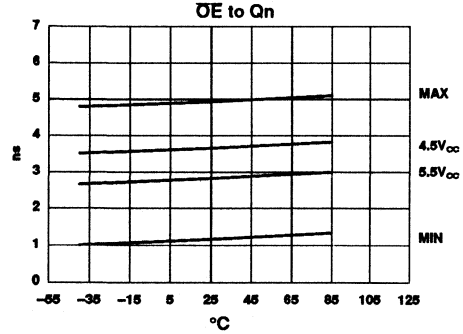
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
CP to Qn



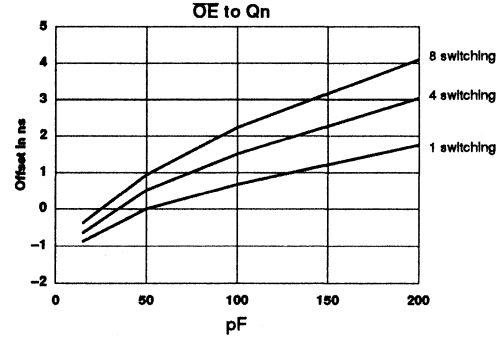
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
CP to Qn



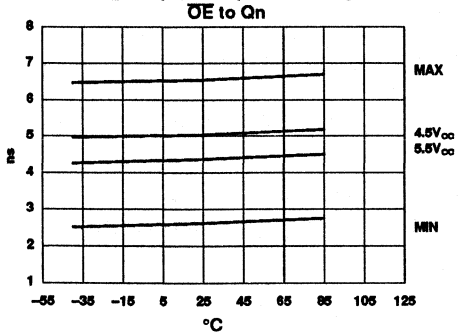
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to Qn



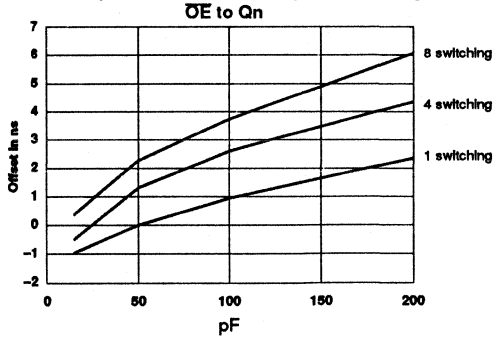
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to Qn



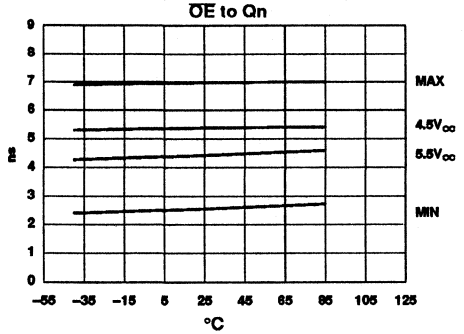
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to Qn



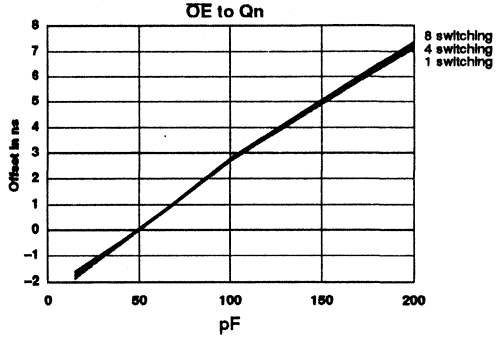
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to Qn



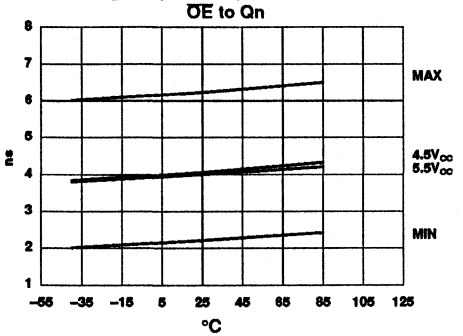
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to Qn



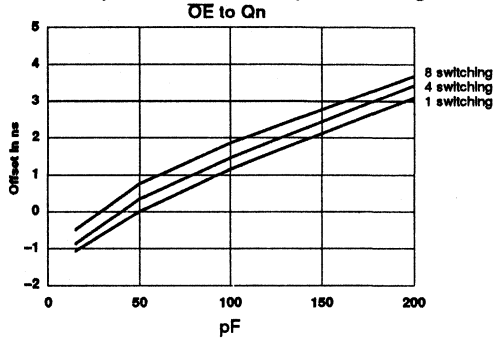
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to Qn



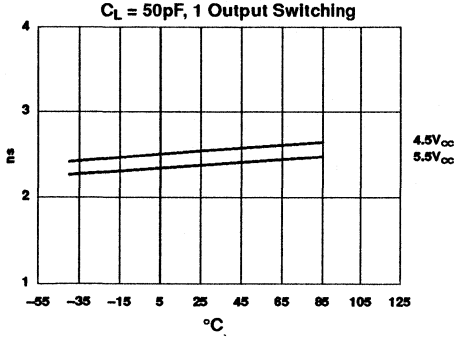
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to Qn



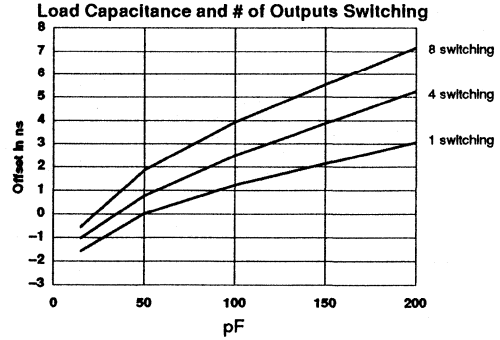
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to Qn



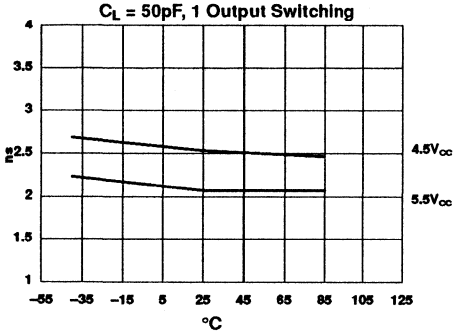
t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



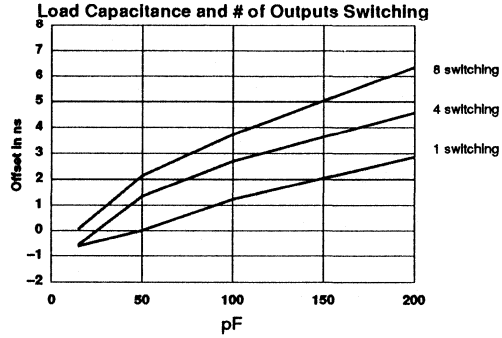
Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching



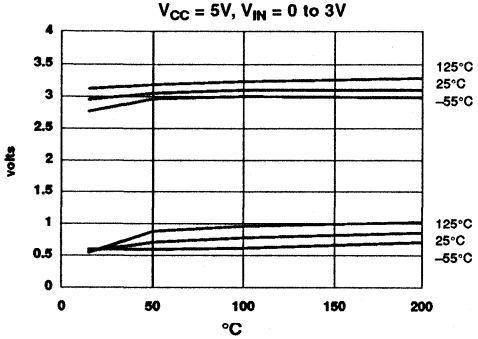
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



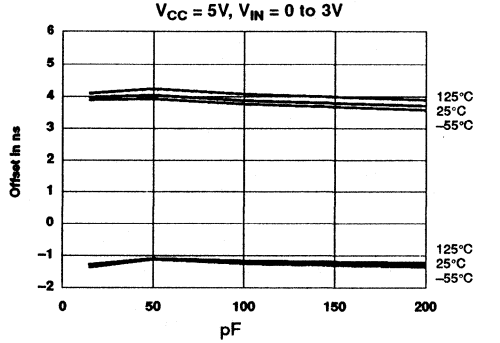
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching



V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



Octal transceiver with dual enable, inverting — 74ABT620

FEATURES

- Octal bidirectional bus interface
- 3-State buffer outputs sink 64mA and source 32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT620 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT620 device is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions. The 74ABT620 is designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs ($\overline{OEBA}$ and OEAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn, or Bn to An	C_L = 50pF; V_{CC} = 5V	3.5	ns
C_{IN}	Input capacitance OE, $\overline{OE}$	V_I = 0V or V_{CC}	4	pF
C_{OUT}	I/) capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

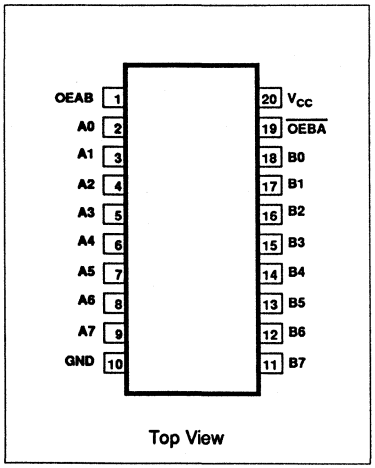
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT620N
20-pin plastic SOL	-40°C to +85°C	74ABT620D

PIN DESCRIPTION

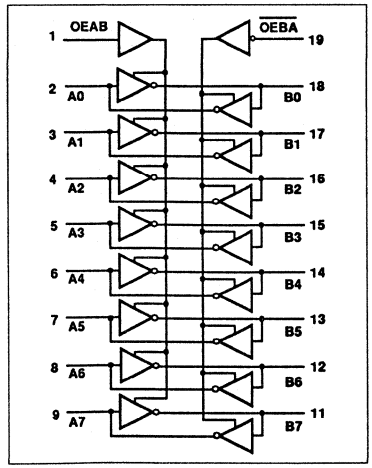
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	Output Enable input
2, 3, 4, 5 6, 7, 8, 9	A0 - A7	Data inputs/outputs (A side)
18, 17, 16, 15 14, 13, 12, 11	B0 - B7	Data inputs/outputs (B side)
19	$\overline{OEBA}$	Ouput Enable input
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

PIN CONFIGURATION

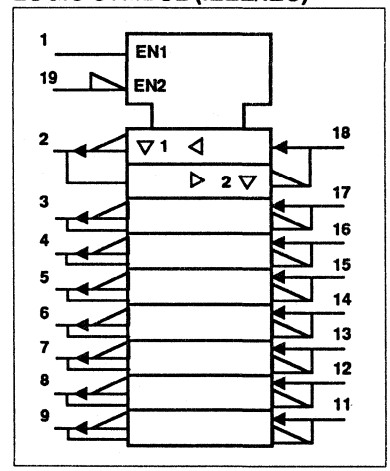


Top View

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		INPUTS / OUTPUTS	
$\overline{OEBA}$	OEAB	An	Bn
L	L	$\overline{B}n$	Inputs
H	H	Inputs	$\overline{A}n$
H	L	Z	Z
L	H	$\overline{B}n$ or Inputs	Inputs $\overline{A}n$

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
			Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
			Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Octal transceiver with dual enable, non-inverting (3-State) 74ABT623

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: +64 mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT623 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT623 device is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The 74ABT623 is designed for asynchronous two-way communication between data buses.

(continued)

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OEBA}$	OEAB	An	Bn
L	L	A = B	Inputs
H	H	Inputs	B = A
H	L	Z	Z
L	H	A=B	B=A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn, or Bn to An	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{OExx}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O pin capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

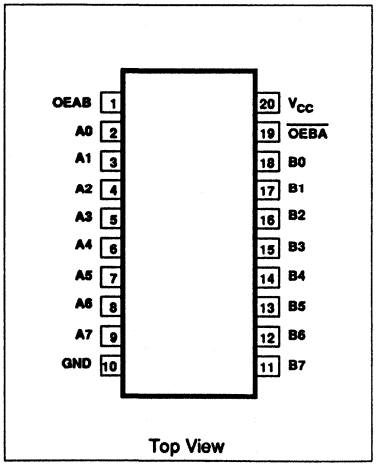
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT623N
20-pin plastic SOL	-40°C to +85°C	74ABT623D

PIN DESCRIPTION

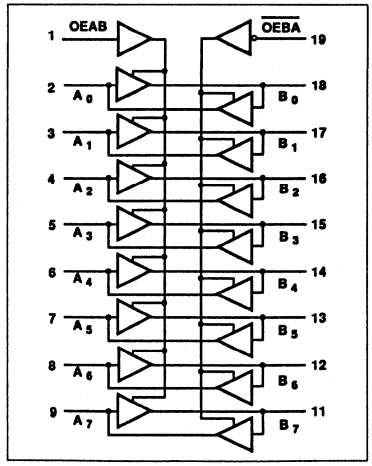
PIN NUMBER	SYMBOL	FUNCTION
1	OEAB	Output Enable input
2, 3, 4, 5 6, 7, 8, 9	A0 - A7	Data inputs/outputs (A side)
18, 17, 16, 15 14, 13, 12, 11	B0 - B7	Data inputs/outputs (B side)
19	$\overline{OEBA}$	Ouput Enable input
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

PIN CONFIGURATION

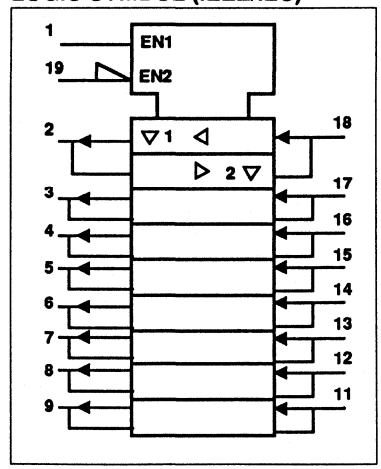


Top View

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



The control function implementation allows for maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs ($\overline{OEBA}$ and OEAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
			Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
			Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Octal transceiver with dual enable, non-inverting (3-State) 74ABT623

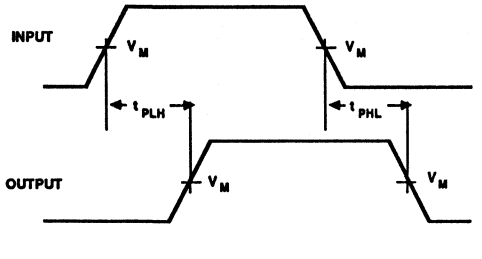
AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

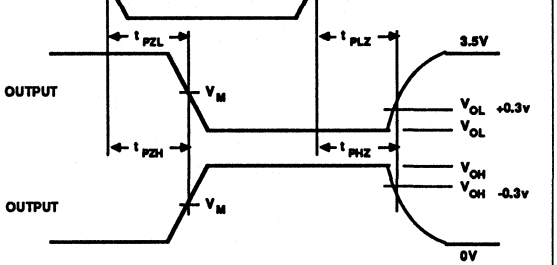
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40° C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.0 1.0	2.8 2.9	4.1 4.2	1.0 1.0	4.6 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.7 1.7	4.8 4.9	6.5 6.5	1.7 1.7	7.5 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.7 1.7	5.0 5.0	6.5 6.5	1.7 1.7	7.5 7.5	ns

AC WAVEFORMS

(V_M = 1.5V, V_{IN} = GND to 3.0V)

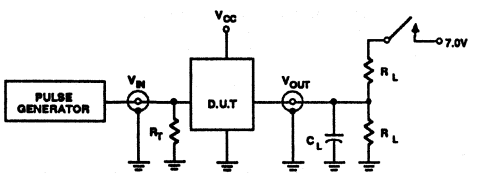


Waveform 1. Waveforms Showing the Input to Output Propagation Delays

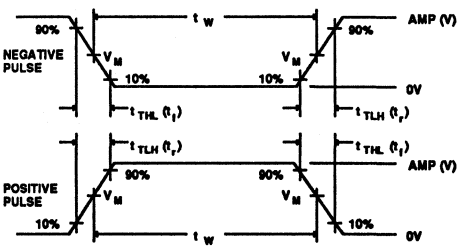


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

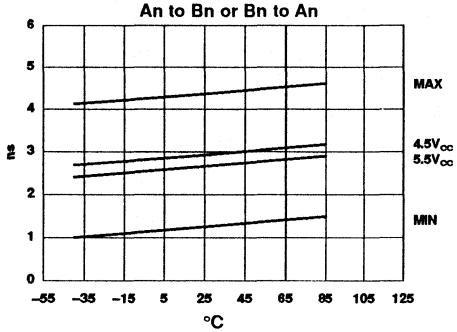
R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

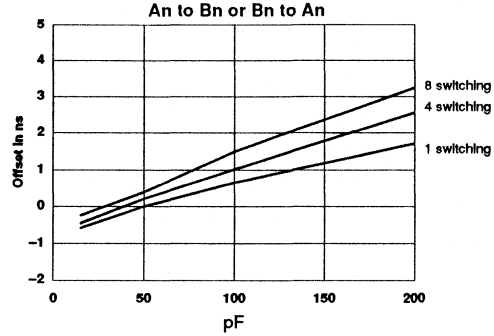
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

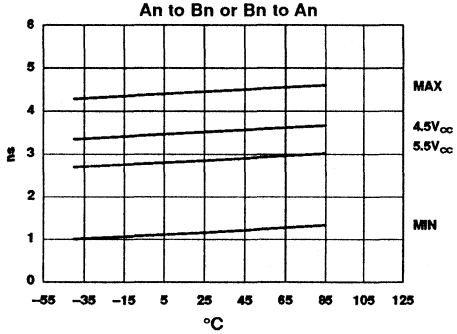
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
An to Bn or Bn to An



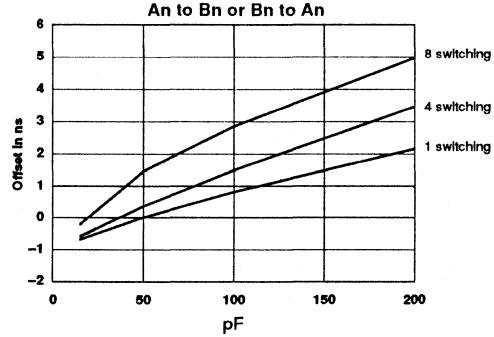
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
An to Bn or Bn to An



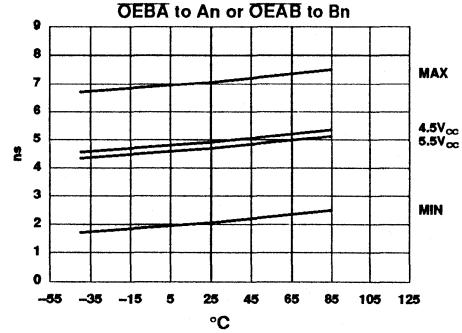
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
An to Bn or Bn to An



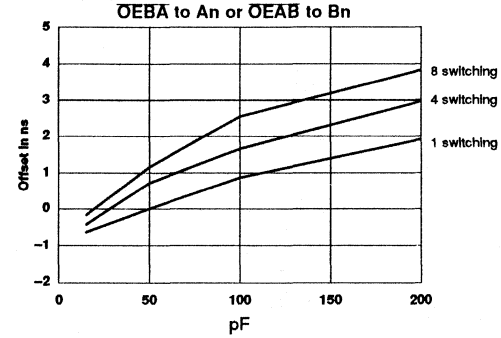
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
An to Bn or Bn to An



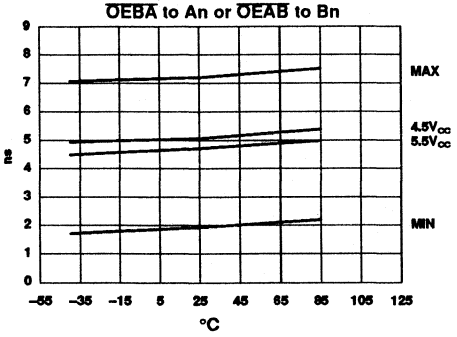
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



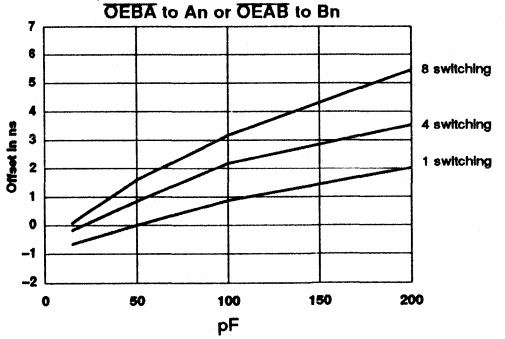
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



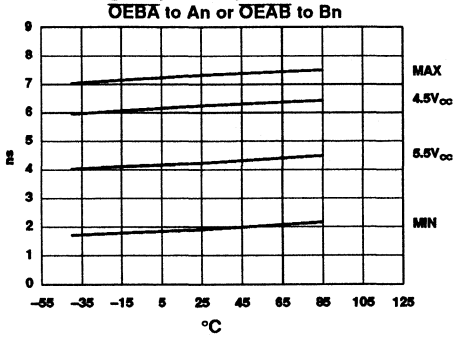
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



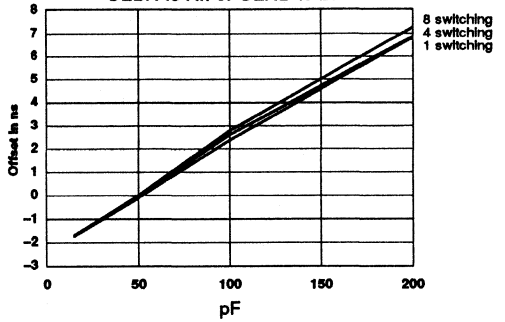
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



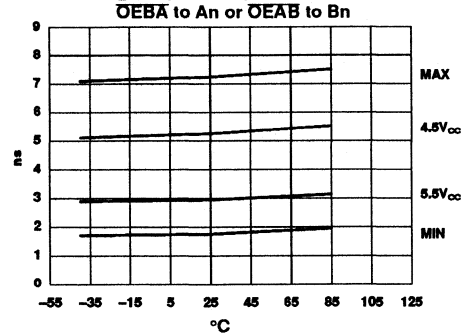
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



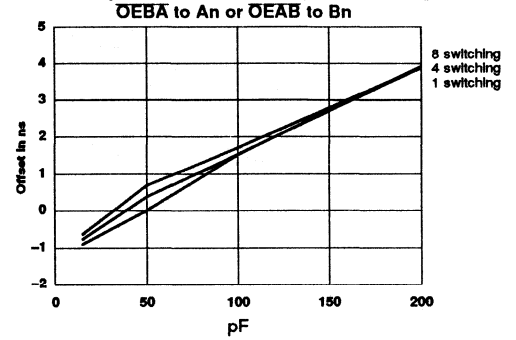
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



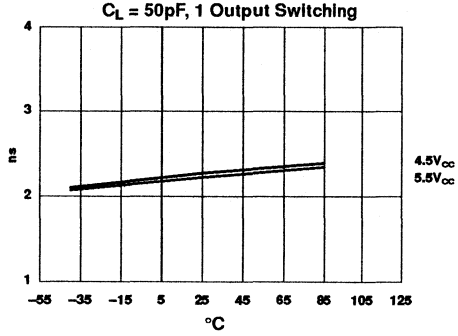
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



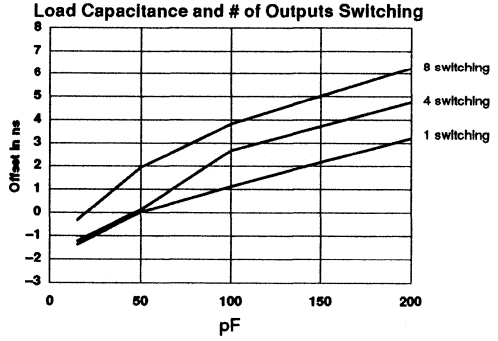
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



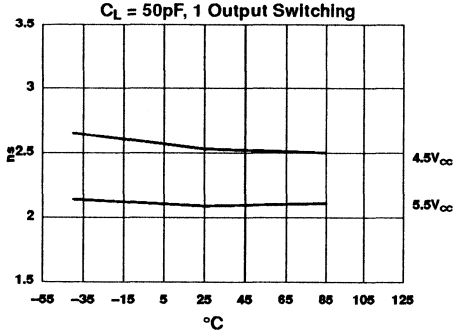
t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



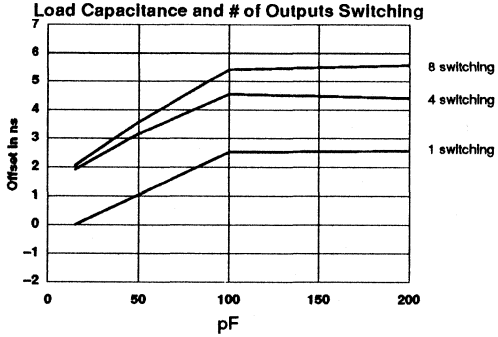
Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching



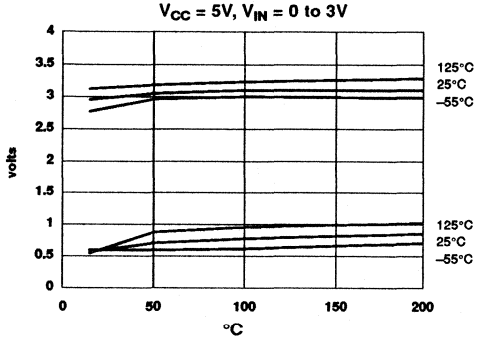
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



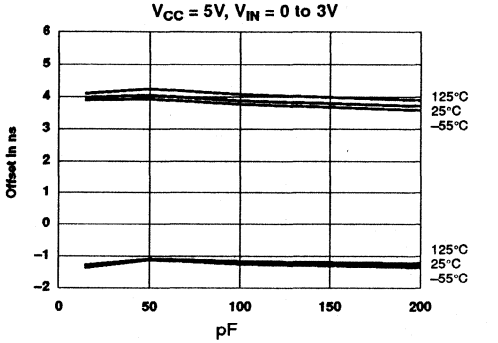
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching



V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



Octal transceiver with direction pin, inverting (3-State) — 74ABT640

FEATURES

- Octal bidirectional bus interface
- Output capability: +64 mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT640 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT640 device is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	An	Bn
L	L	$\overline{B}n$	Inputs
L	H	Inputs	$\overline{A}n$
H	X	Z	Z

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn, or Bn to An	CL = 50pF; V_{CC} = 5V	3.5	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	VI = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	VI = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

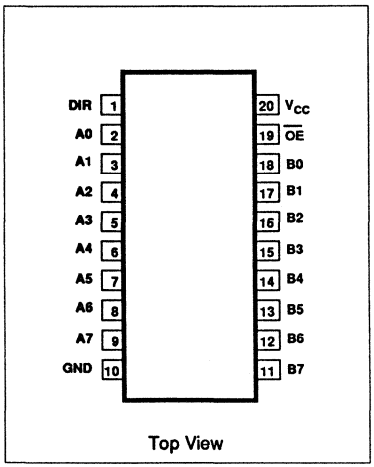
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT640N
20-pin plastic SOL	-40°C to +85°C	74ABT640D

PIN DESCRIPTION

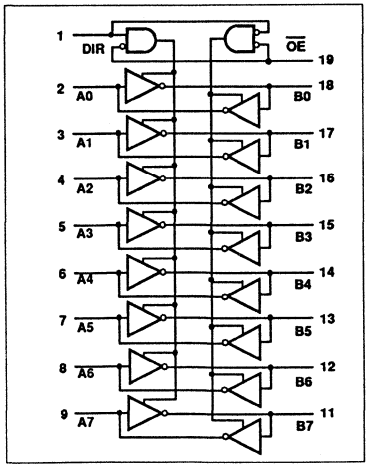
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	DIR	Direction control input
2, 3, 4, 5 6, 7, 8, 9	A0 - A7	Data inputs/outputs (A side)
18, 17, 16, 15 14, 13, 12, 11	B0 - B7	Data inputs/outputs (B side)
19	$\overline{OE}$	Ouput enable
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

PIN CONFIGURATION

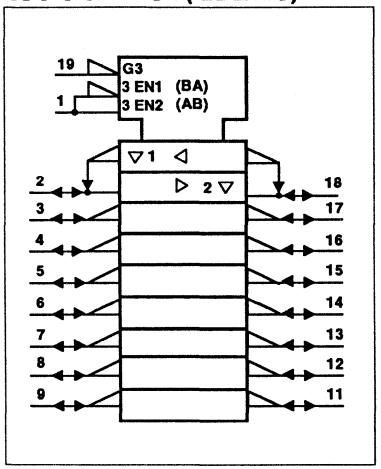


Top View

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
I_{IH} + I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
			Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
			Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Octal bus transceiver/register (3-State) 74ABT646

FEATURES

- Combines 'ABT245 and 'ABT374 type functions in one device
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Outputs sink 64mA and source 32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT646 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT646 Transceiver/Register consists of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) pins determine whether data is stored or transferred through the device in real-time. The DIR determines which bus will receive data when the $\overline{OE}$ is active Low. In the isolation mode ($\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn, or Bn to An	C_L = 50pF; V_{CC} = 5V	4.4	ns
C_{IN}	Input capacitance CP, S, $\overline{OE}$	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

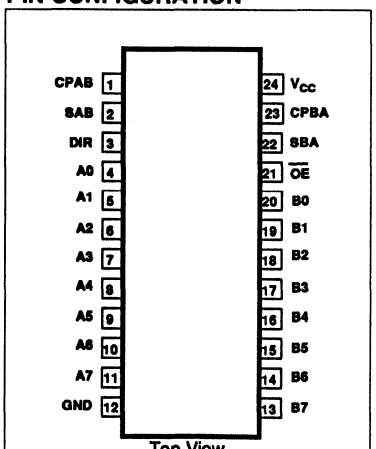
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT646N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT646D

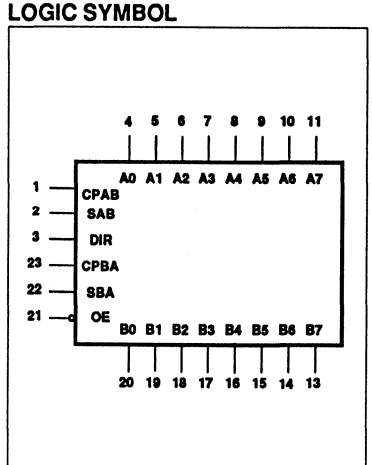
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1,23	CPAB / CPBA	Clock input A to B / Clock input B to A
2, 22	SAB / SBA	Select input A to B / Select input B to A
3	DIR	Direction control input
4, 5, 6, 7 8, 9, 10, 11	A0 - A7	Data inputs/outputs (A side)
20, 19, 18, 17 16, 15, 14, 13	B0 - B7	Data inputs/outputs (B side)
21	$\overline{OE}$	Output enable input
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

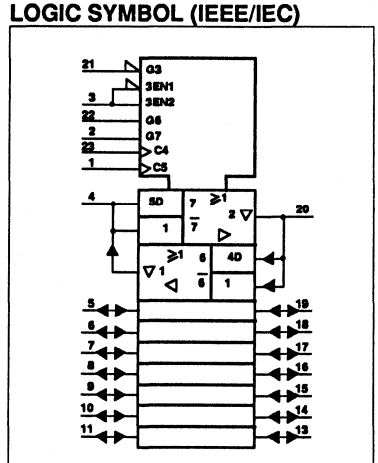
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

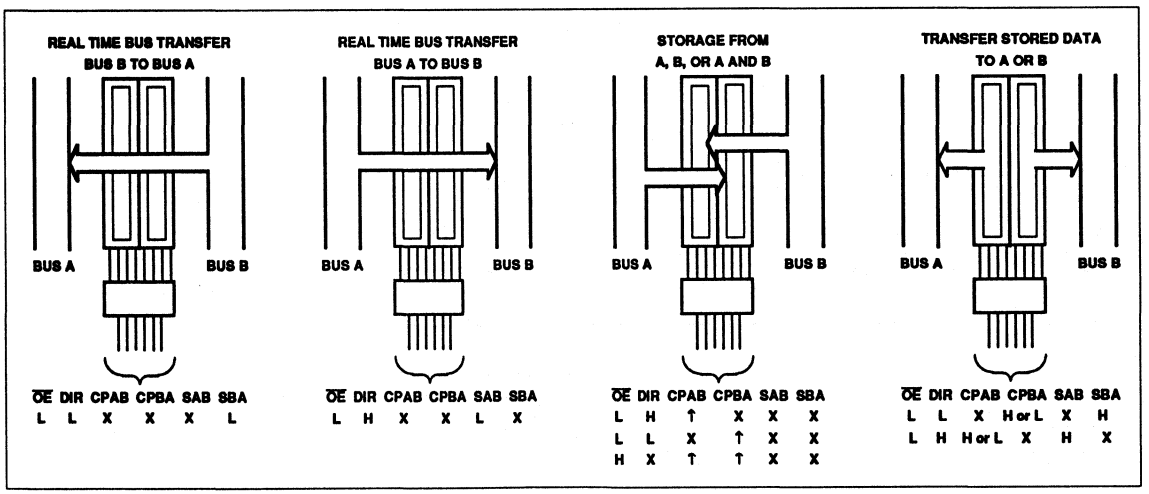


and transmit data. Only one of the two buses, A or B may be driven at a time. The following examples demonstrate the four fundamental bus management functions that can be performed with the 74ABT646.

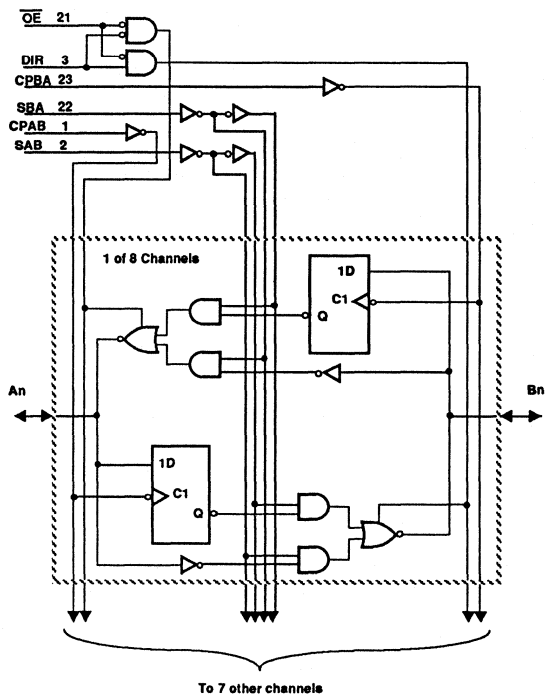
FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	A0-A7	B0-B7	
X	X	↑	X	X	X	Input	Unspecified*	Store A, B unspecified*
X	X	X	↑	X	X	Unspecified*	Input	Store B, A unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X			Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real time B data to A bus
L	L	X	H or L	X	H			Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real time A data to B bus
L	H	H or L	X	H	X			Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to High clock transition
* = The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to High transition of the clock.



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	74ABT646					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40° C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	125	180		125		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	Waveform 1	2.2 1.7	5.3 5.9	6.8 7.4	2.2 1.7	7.8 8.4	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or B_n to An	Waveform 1	1.5 1.5	4.4 4.4	5.9 5.9	1.5 1.5	6.9 6.9	ns
t_{PLH} t_{PHL}	Propagation delay SAB to Bn or SBA to An	Waveform 2, 3	1.5 1.5	4.6 5.4	6.1 6.9	1.5 1.5	7.1 7.9	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to An or Bn	Waveform 2, 3	1.0 2.1	3.8 5.1	5.3 7.4	1.0 2.1	6.3 8.8	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	1.5 1.5	6.2 5.7	7.3 7.0	1.5 1.5	8.3 7.5	ns
t_{PZH} t_{PZL}	Output Enable time DIR to An or Bn	Waveform 5 Waveform 6	1.2 2.5	4.2 5.5	5.7 9.0	1.2 2.5	6.7 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to An or Bn	Waveform 5 Waveform 6	1.5 1.5	5.2 5.7	6.7 7.2	1.5 1.5	7.7 8.2	ns

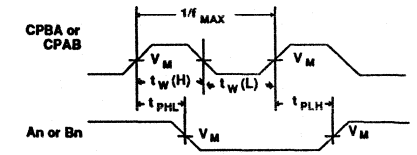
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

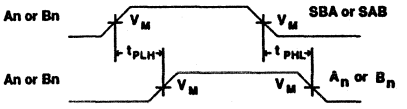
SYMBOL	PARAMETER	WAVEFORM	74ABT646					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40° C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
ts(H) ts(L)	Setup time , High or Low An to CPAB or Bn to CPBA	Waveform 4	3.5 3.0			3.5 3.0		ns
th(H) th(L)	Hold time, High or Low An to CPAB or Bn to CPBA	Waveform 4	0.0 0.0			0.0 0.0		ns
tw(H) tw(L)	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.0 4.0			4.0 4.0		ns

AC WAVEFORMS

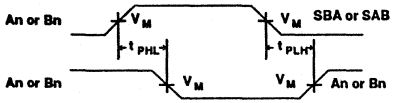
(V_M = 1.5V, V_{IN} = GND to 3.0V)



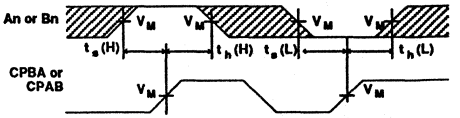
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



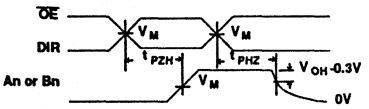
Waveform 2. Propagation Delay, An or Bn to Bn or An and SBA or SAB to An or Bn



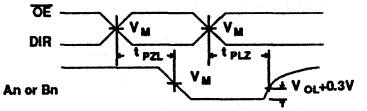
Waveform 3. Propagation Delay, An or Bn to Bn or An and SBA or SAB to An or Bn



Waveform 4. Data Setup And Hold Times



Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level

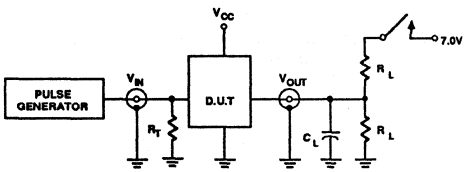


Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

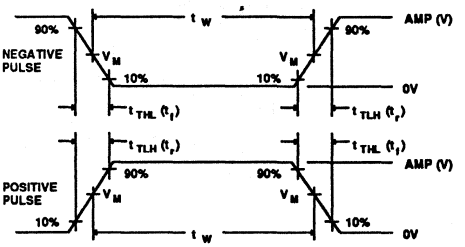
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

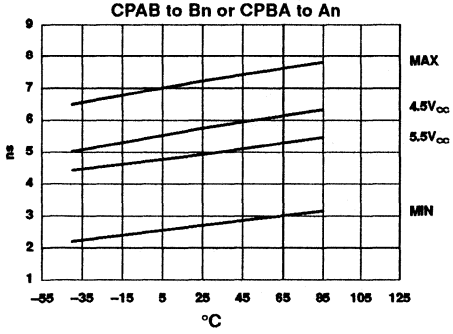


V_M = 1.5V

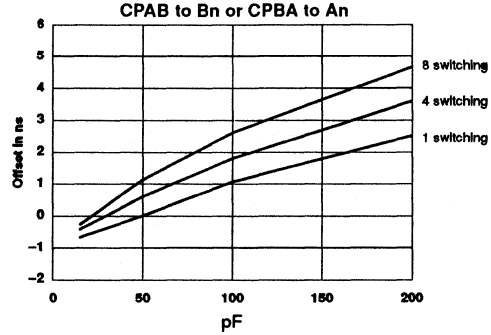
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

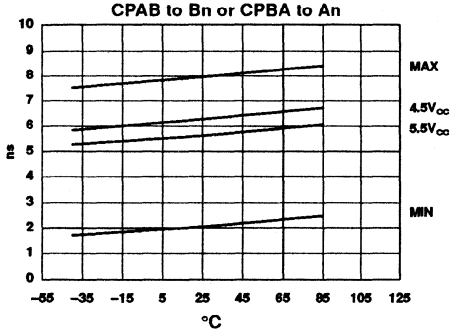
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
CPAB to Bn or CPBA to An



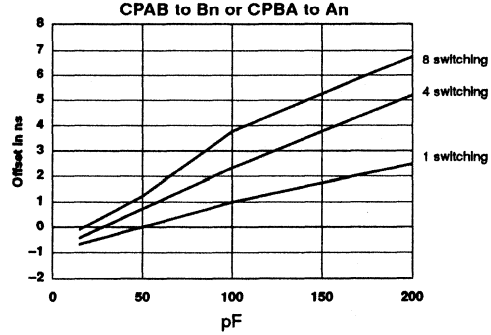
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
CPAB to Bn or CPBA to An



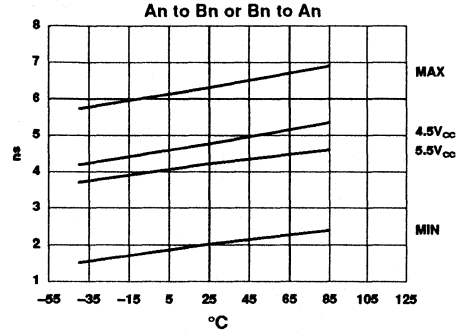
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
CPAB to Bn or CPBA to An



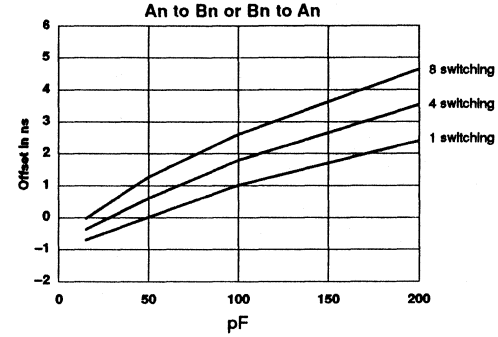
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
CPAB to Bn or CPBA to An



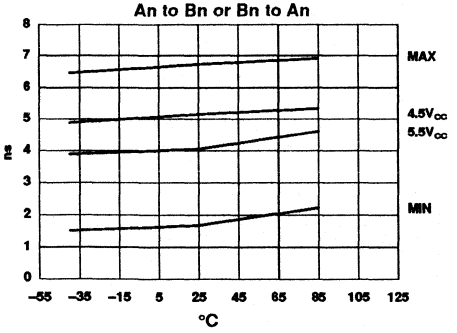
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
An to Bn or Bn to An



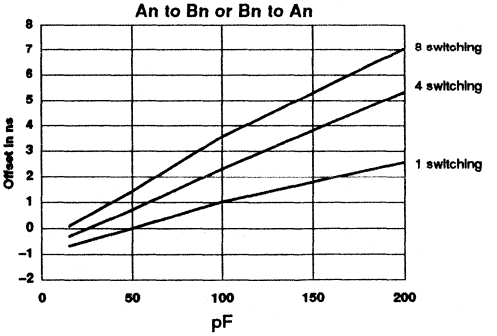
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
An to Bn or Bn to An



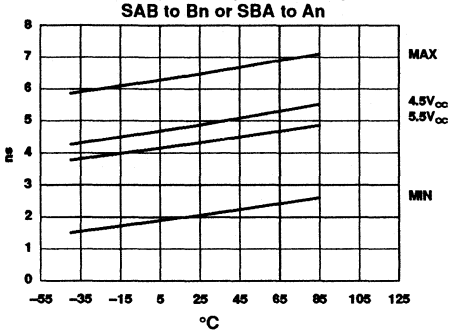
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
An to Bn or Bn to An



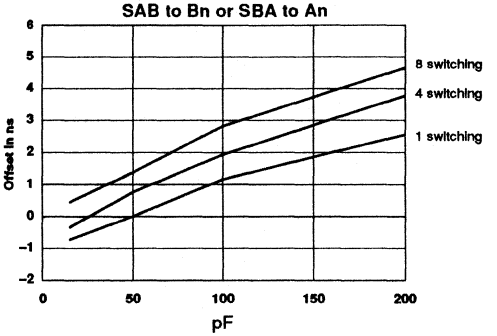
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
An to Bn or Bn to An



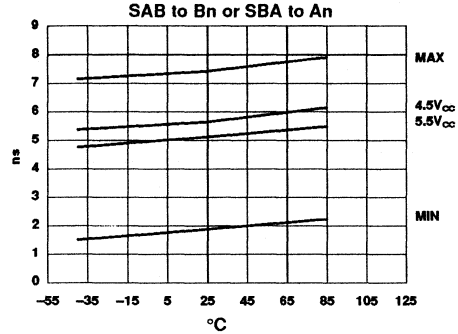
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
SAB to Bn or SBA to An



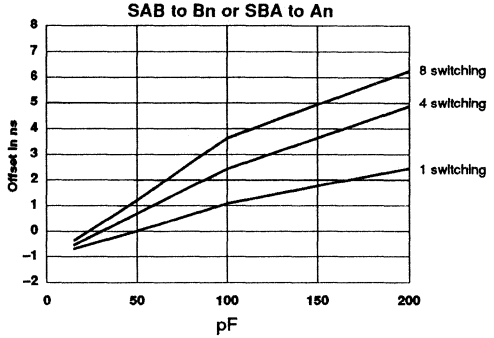
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
SAB to Bn or SBA to An



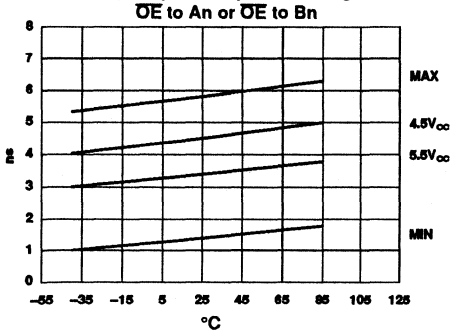
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
SAB to Bn or SBA to An



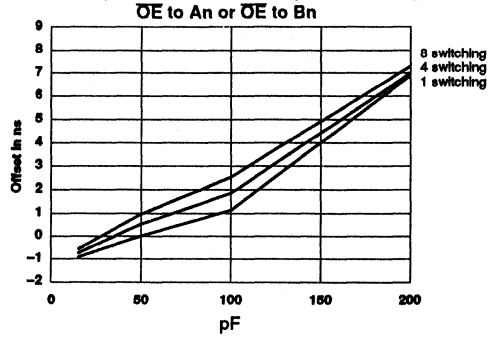
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
SAB to Bn or SBA to An



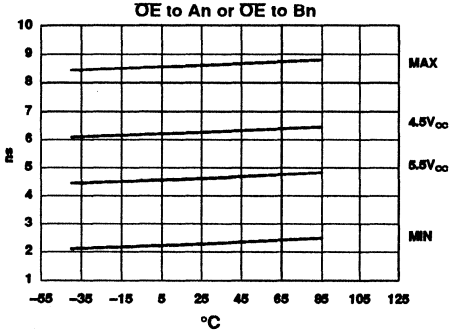
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



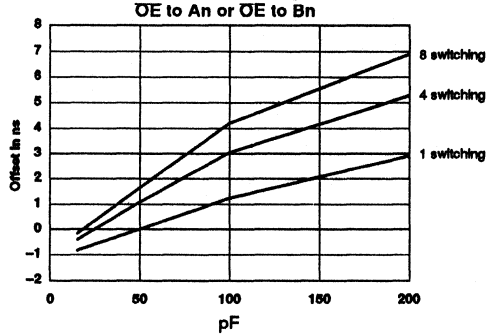
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



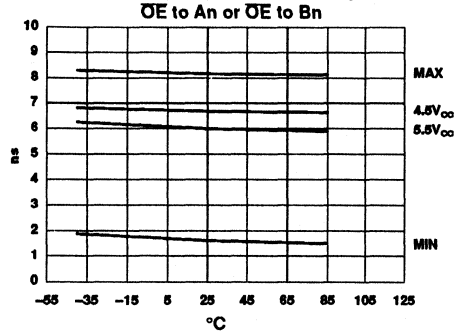
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



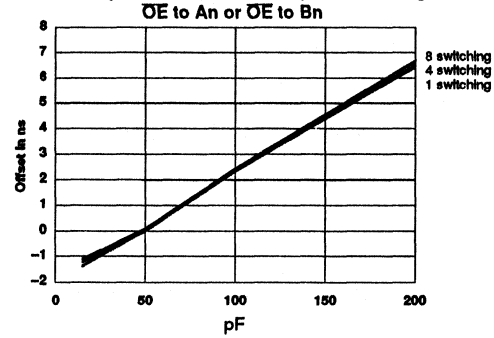
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



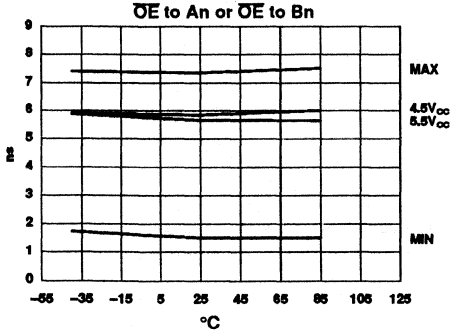
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



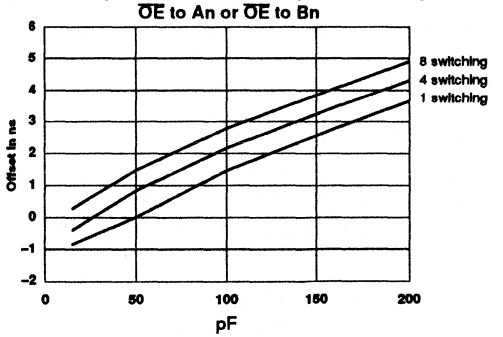
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



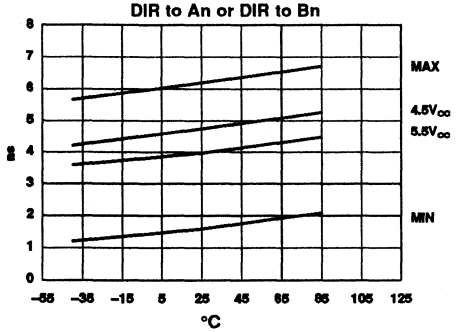
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



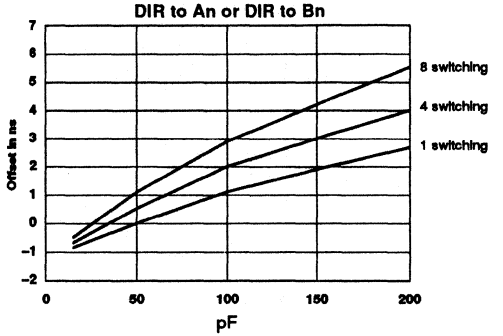
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



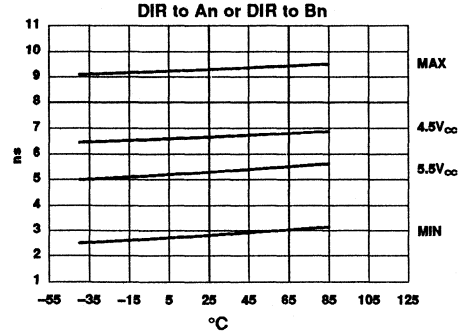
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
DIR to An or DIR to Bn



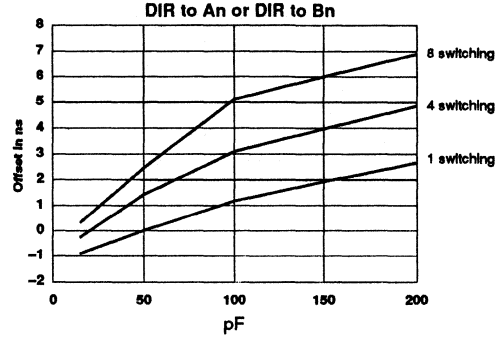
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
DIR to An or DIR to Bn



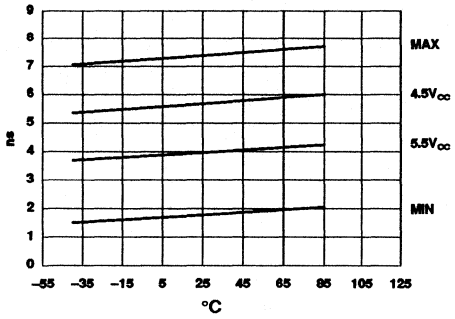
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
DIR to An or DIR to Bn



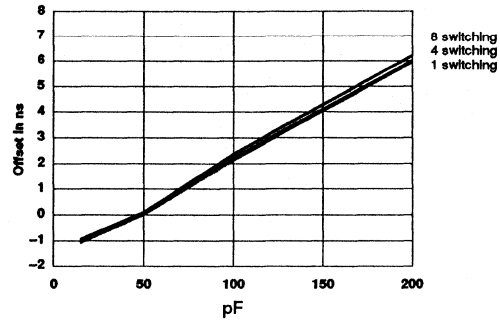
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
DIR to An or DIR to Bn



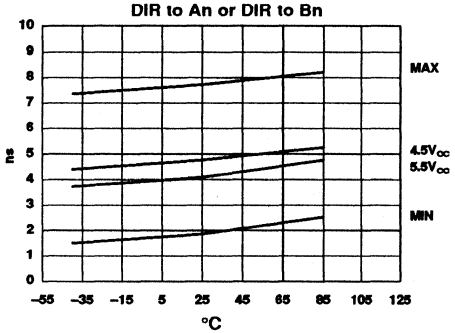
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
DIR to An or DIR to Bn



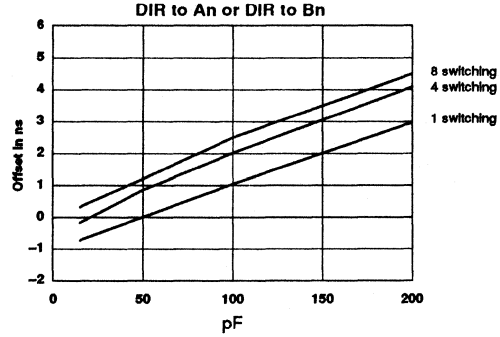
Adjustment of t_{PHZ} for
Load Capacitance/# of Outputs
DIR to An or DIR to Bn



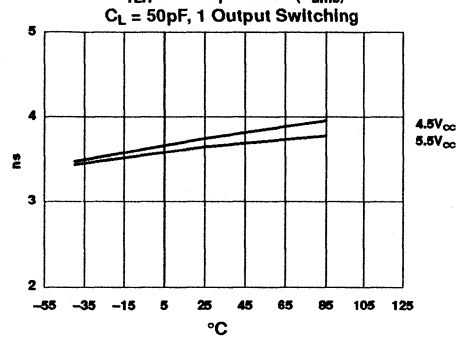
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
DIR to An or DIR to Bn



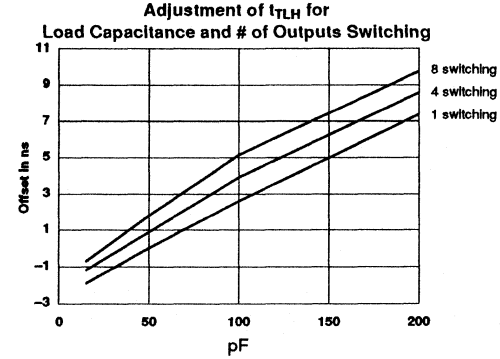
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
DIR to An or DIR to Bn

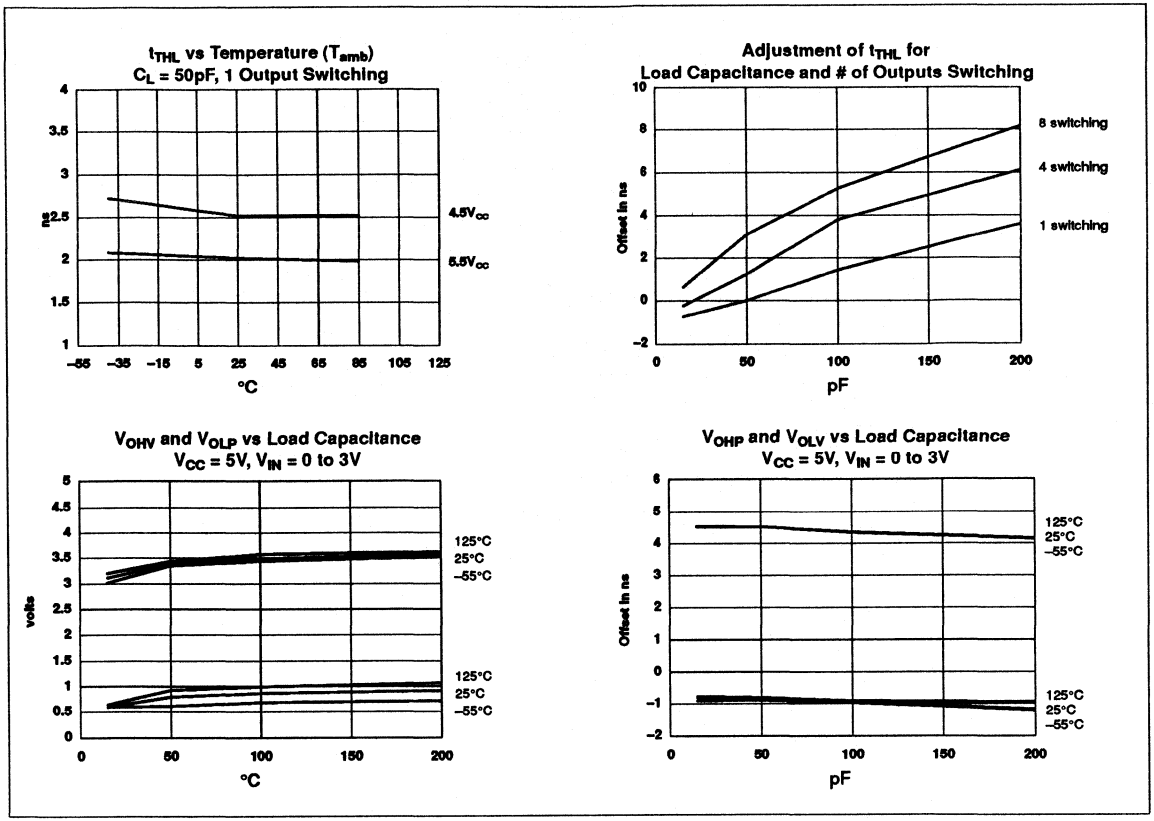


t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching




t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V_{CC}
5.5V_{CC}
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
8 switching
4 switching
1 switching
V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
volts
°C
125°C
25°C
–55°C
V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
Offset in ns
pF
125°C
25°C
–55°C

Octal bus transceiver/register, inverting (3-State)

74ABT648

FEATURES

- Combines 74ABT245 and 74ABT374 type functions in one device
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT648 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT648 Transceiver/Register consists of bus transceiver circuits with Inverting 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay $\overline{An}$ to $\overline{Bn}$, or $\overline{Bn}$ to $\overline{An}$	C_L = 50pF; V_{CC} = 5V	5.9	ns
C_{IN}	Input capacitance CP, S, $\overline{OE}$, DIR	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

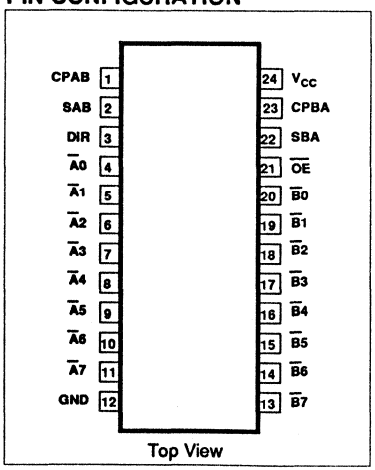
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT648N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT648D

PIN DESCRIPTION

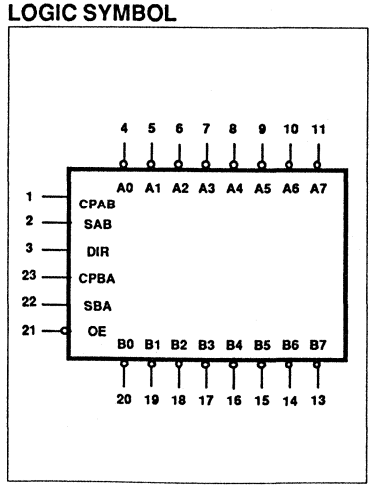
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1,23	CPAB / CPBA	Clock input A to B / Clock input B to A
2, 22	SAB / SBA	Select input A to B / Select input B to A
3	DIR	Direction control input
4, 5, 6, 7 8, 9, 10, 11	$\overline{A0}$ - $\overline{A7}$	Data inputs/outputs (A side)
20, 19, 18, 17 16, 15, 14, 13	$\overline{B0}$ - $\overline{B7}$	Data inputs/outputs (B side)
21	$\overline{OE}$	Ouput enable input
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

PIN CONFIGURATION

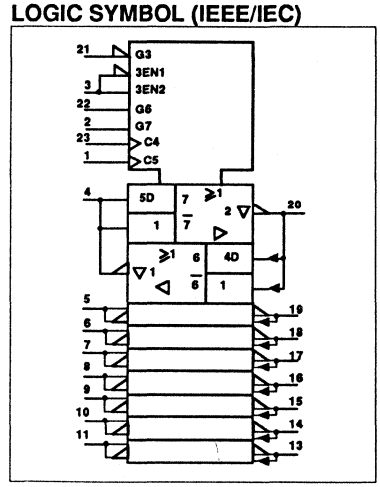


Top View

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



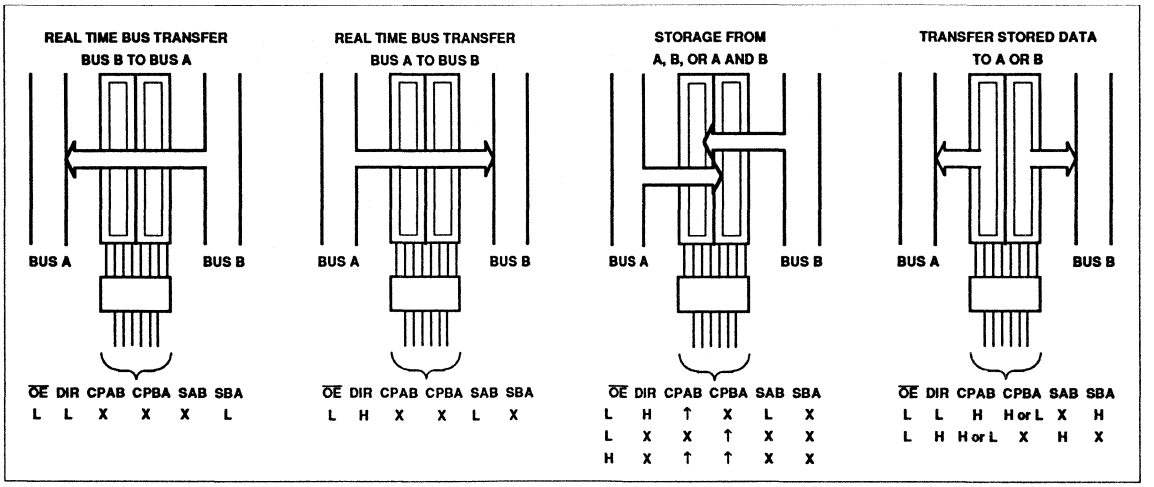
Octal bus transceiver/register, inverting (3-State) 74ABT648

The select (SAB, SBA) pins determine whether data is stored or transferred through the device in real-time. The DIR determines which bus will receive data when the $\overline{OE}$ is active Low. In the isolation mode ($\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. Outputs from real-time, or stored register will be inverted. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time. The following examples demonstrate the four fundamental bus management functions that can be performed with the 74ABT648.

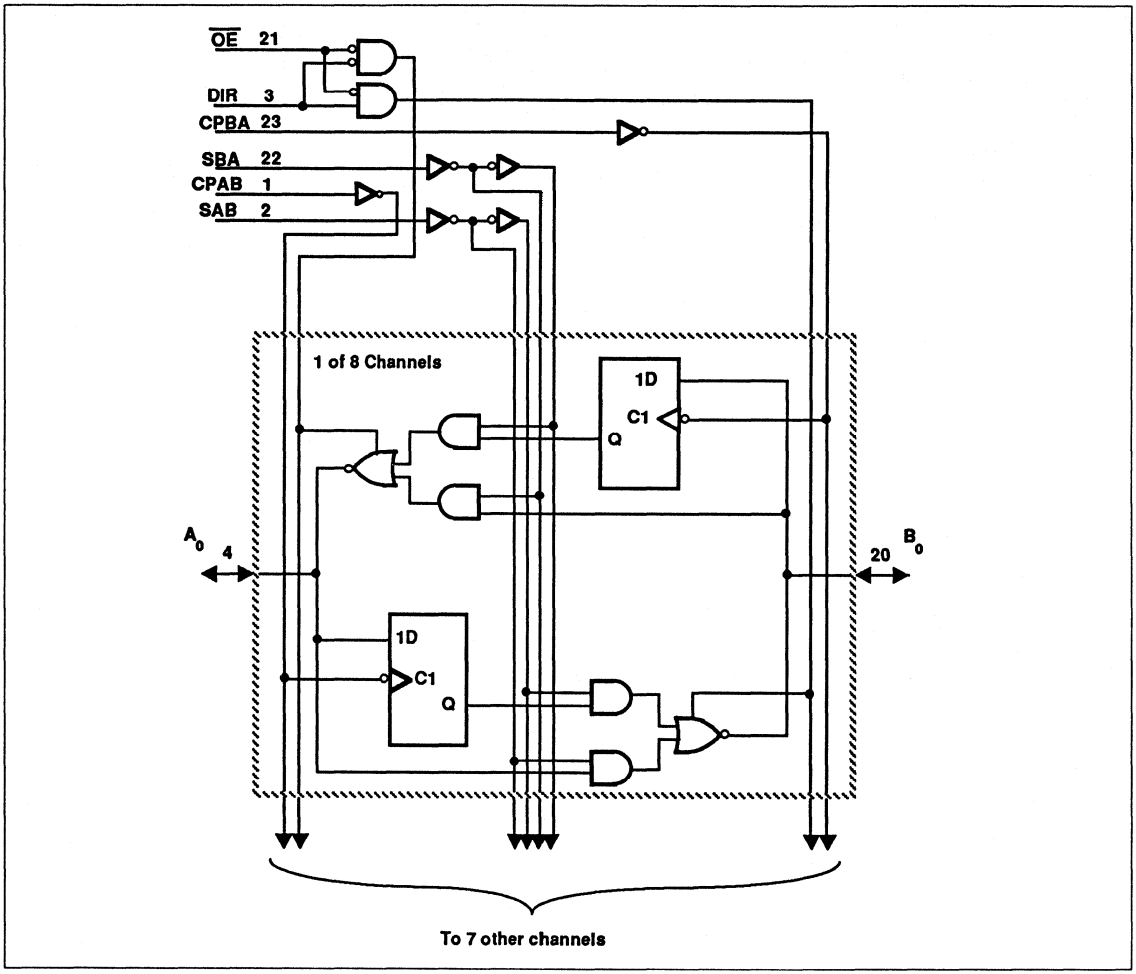
FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
OE	DIR	CPAB	CPBA	SAB	SBA	A0-A7	B0-B7	
X	X	↑	X	X	X	Input	Unspecified*	Store A, B unspecified*
X	X	X	↑	X	X	Unspecified*	Input	Store B, A unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X			Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real time $\overline{B}$ data to A bus
L	L	X	H or L	X	H			Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real time $\overline{A}$ data to B bus
L	H	H or L	X	H	X			Stored $\overline{A}$ data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑= Low-toHigh clock transition
* = The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled,i.e., data at the bus pins will be stored on every Low-toHigh transition of the clock.



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
I_{IH} + I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	74ABT648					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40° C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	125	200		125		Mhz
t_{PLH} t_{PHL}	Propagation delay CPAB to $\overline{Bn}$ or CPBA to $\overline{An}$	Waveform 1	2.2 3.1	5.3 5.9	6.8 7.4	2.2 3.1	7.8 8.4	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or $\overline{Bn}$ to $\overline{An}$	Waveform 2, 3	1.0 1.7	3.5 4.2	5.0 5.5	1.0 1.7	6.0 6.2	ns
t_{PLH} t_{PHL}	Propagation delay SAB to $\overline{Bn}$ or SBA to $\overline{An}$	Waveform 2, 3	1.7 2.5	4.6 5.3	5.9 6.8	1.7 2.5	6.9 7.8	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to $\overline{An}$ or $\overline{Bn}$	Waveform 5 Waveform 6	1.4 2.7	3.8 5.1	5.3 6.4	1.4 2.7	6.3 7.5	ns
t_{PZH} t_{PZL}	Output Enable time DIR to $\overline{An}$ or $\overline{Bn}$	Waveform 5 Waveform 6	1.9 2.9	4.2 5.6	5.4 6.9	1.9 2.9	6.4 7.8	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to $\overline{An}$ or $\overline{Bn}$	Waveform 5 Waveform 6	4.2 3.7	6.2 5.7	7.3 7.0	4.2 3.7	8.3 7.5	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to $\overline{An}$ or $\overline{Bn}$	Waveform 5 Waveform 6	2.1 2.1	4.2 4.5	6.7 7.2	2.1 2.1	7.4 8.2	ns

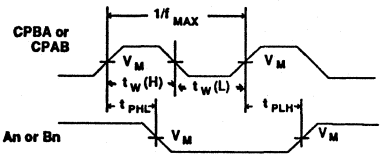
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

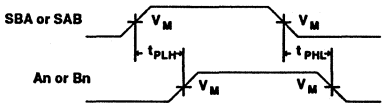
SYMBOL	PARAMETER	WAVEFORM	74ABT648					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40° C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time , High or Low $\overline{An}$ to CPAB or $\overline{Bn}$ to CPBA	Waveform 4	3.0 2.5	1.5 1.0		3.0 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{An}$ to CPAB or $\overline{Bn}$ to CPBA	Waveform 4	0.0 0.0	-1.0 -1.0		0.0 0.0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	3.5 4.0	2.5 3.0		3.5 4.0		ns

AC WAVEFORMS

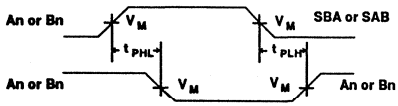
(V_M = 1.5V, V_{IN} = GND to 3.0V)



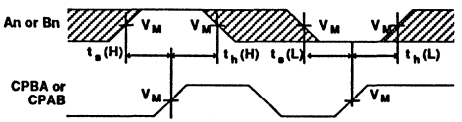
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



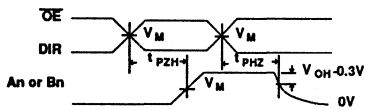
Waveform 2. Propagation Delay, An or Bn to Bn or An and SBA or SAB to An or Bn



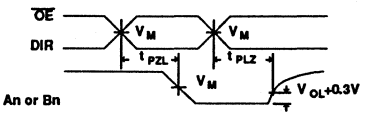
Waveform 3. Propagation Delay, An or Bn to Bn or An and SBA or SAB to An or Bn



Waveform 4. Data Setup And Hold Times



Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level

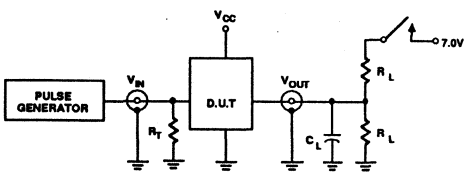


Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V

The shaded areas indicste when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

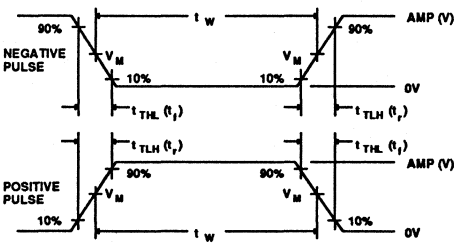
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

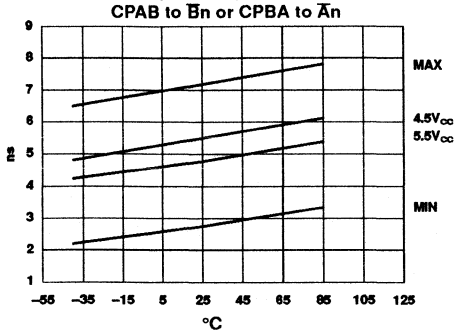


V_M = 1.5V

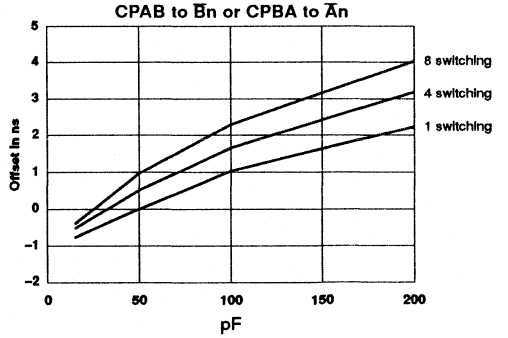
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

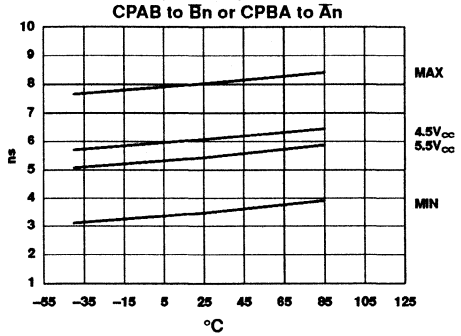
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
CPAB to $\overline{B}$n or CPBA to $\overline{A}$n



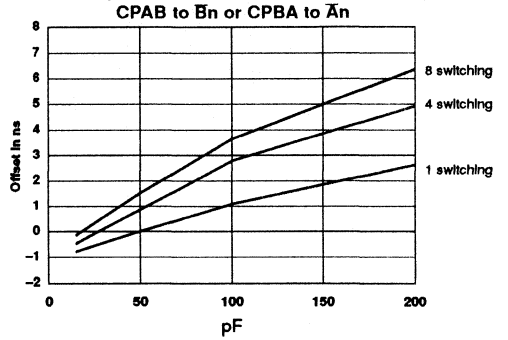
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
CPAB to $\overline{B}$n or CPBA to $\overline{A}$n



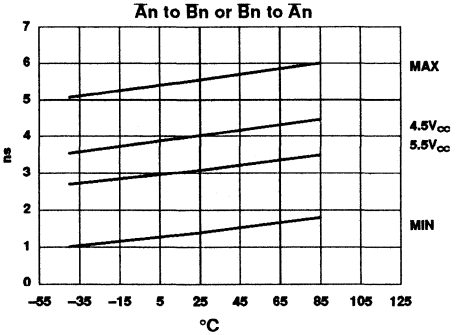
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
CPAB to $\overline{B}$n or CPBA to $\overline{A}$n



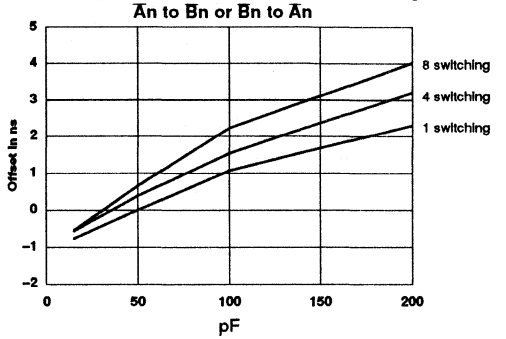
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
CPAB to $\overline{B}$n or CPBA to $\overline{A}$n



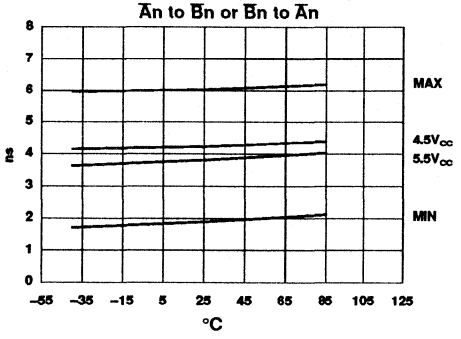
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{A}$n to $\overline{B}$n or $\overline{B}$n to $\overline{A}$n



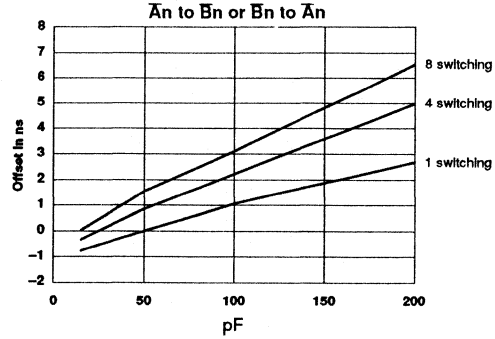
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
$\overline{A}$n to $\overline{B}$n or $\overline{B}$n to $\overline{A}$n



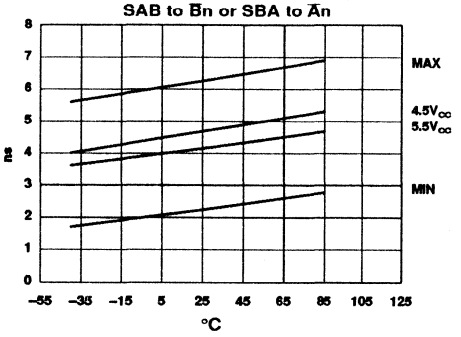
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{A}n$ to $\overline{B}n$ or $\overline{B}n$ to $\overline{A}n$



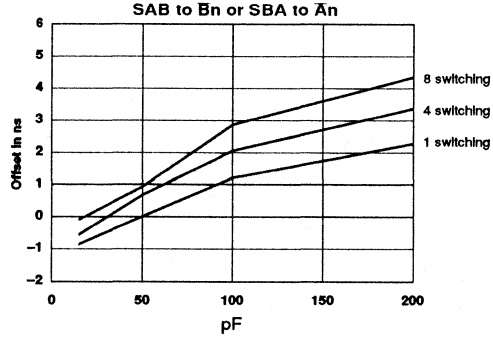
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
$\overline{A}n$ to $\overline{B}n$ or $\overline{B}n$ to $\overline{A}n$



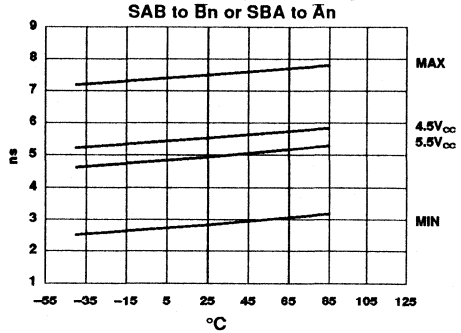
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
SAB to $\overline{B}n$ or SBA to $\overline{A}n$



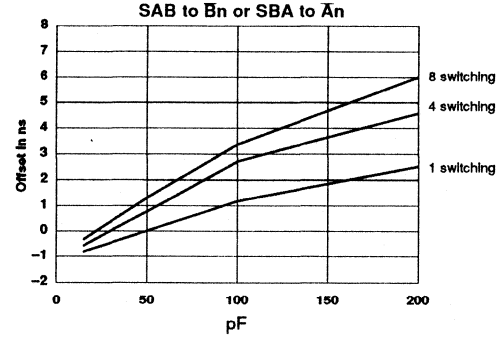
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
SAB to $\overline{B}n$ or SBA to $\overline{A}n$



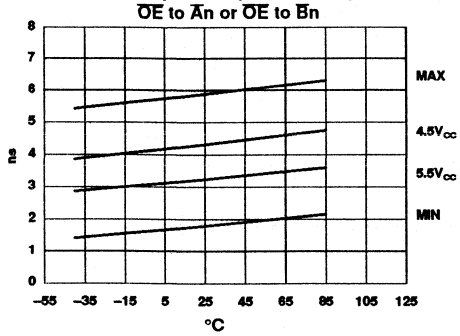
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
SAB to $\overline{B}n$ or SBA to $\overline{A}n$



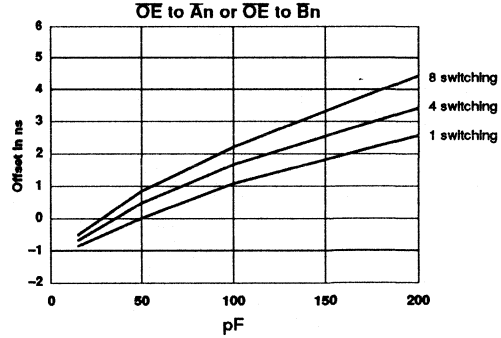
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
SAB to $\overline{B}n$ or SBA to $\overline{A}n$



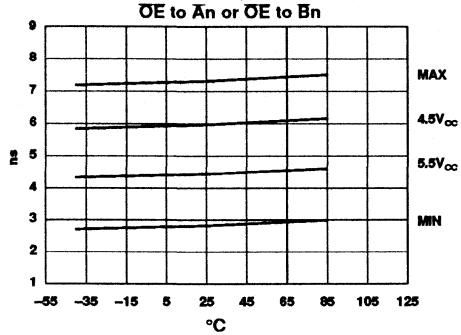
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to $\overline{An}$ or $\overline{OE}$ to $\overline{Bn}$



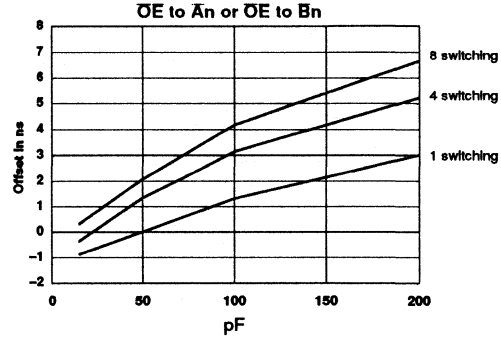
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to $\overline{An}$ or $\overline{OE}$ to $\overline{Bn}$



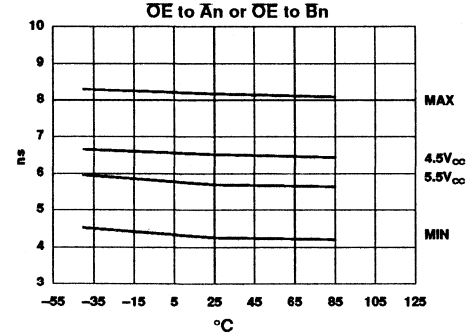
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to $\overline{An}$ or $\overline{OE}$ to $\overline{Bn}$



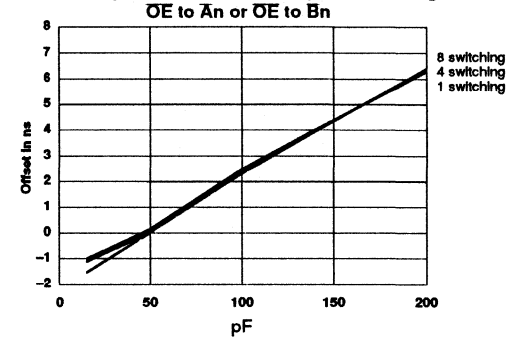
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to $\overline{An}$ or $\overline{OE}$ to $\overline{Bn}$



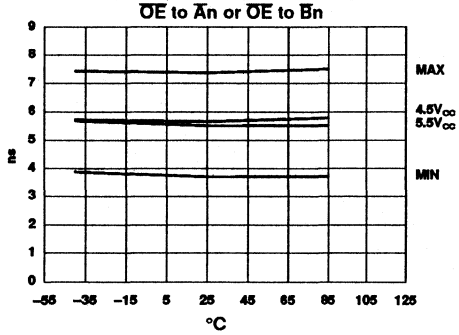
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to $\overline{An}$ or $\overline{OE}$ to $\overline{Bn}$



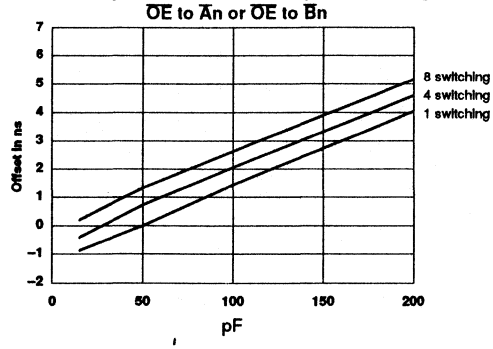
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to $\overline{An}$ or $\overline{OE}$ to $\overline{Bn}$



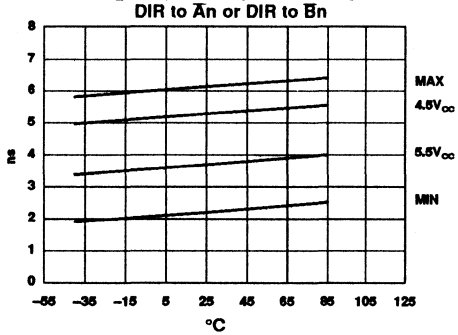
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to $\overline{An}$ or $\overline{OE}$ to $\overline{Bn}$



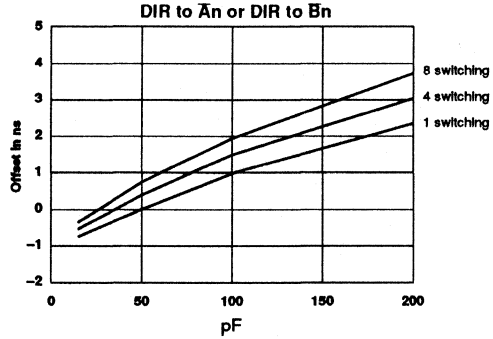
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to $\overline{An}$ or $\overline{OE}$ to $\overline{Bn}$



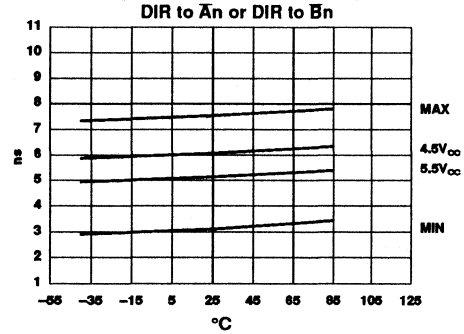
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
DIR to $\overline{An}$ or DIR to $\overline{Bn}$



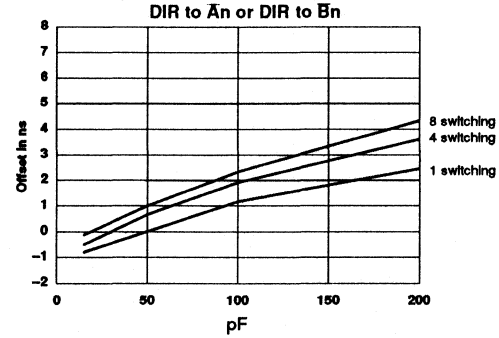
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
DIR to $\overline{An}$ or DIR to $\overline{Bn}$



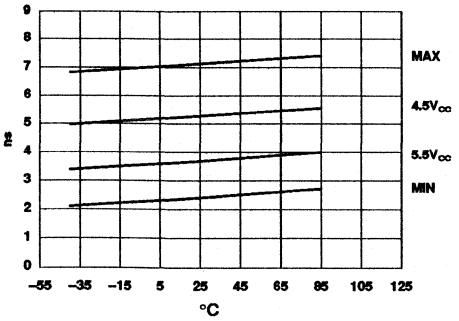
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
DIR to $\overline{An}$ or DIR to $\overline{Bn}$



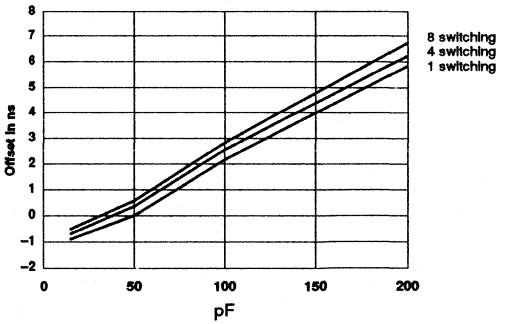
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
DIR to $\overline{An}$ or DIR to $\overline{Bn}$



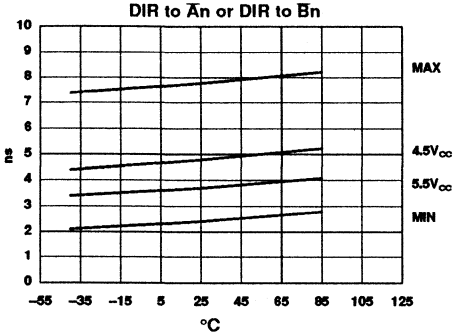
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
DIR to $\overline{A}$n or DIR to $\overline{B}$n



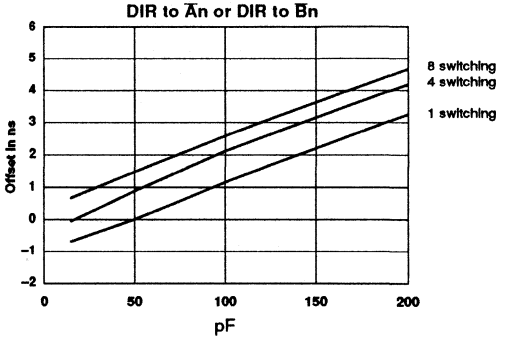
Adjustment of t_{PHZ} for
Load Capacitance/# of Outputs
DIR to $\overline{A}$n or DIR to $\overline{B}$n



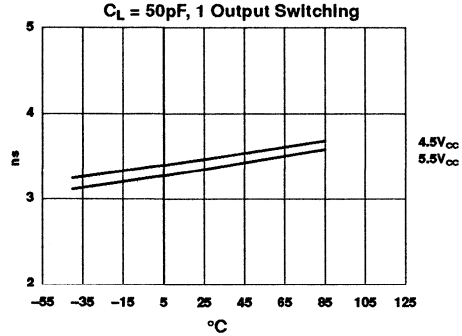
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
DIR to $\overline{A}$n or DIR to $\overline{B}$n



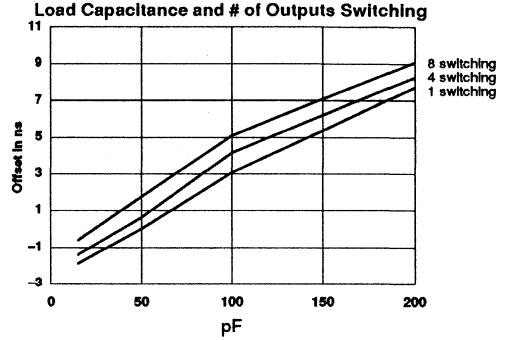
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
DIR to $\overline{A}$n or DIR to $\overline{B}$n

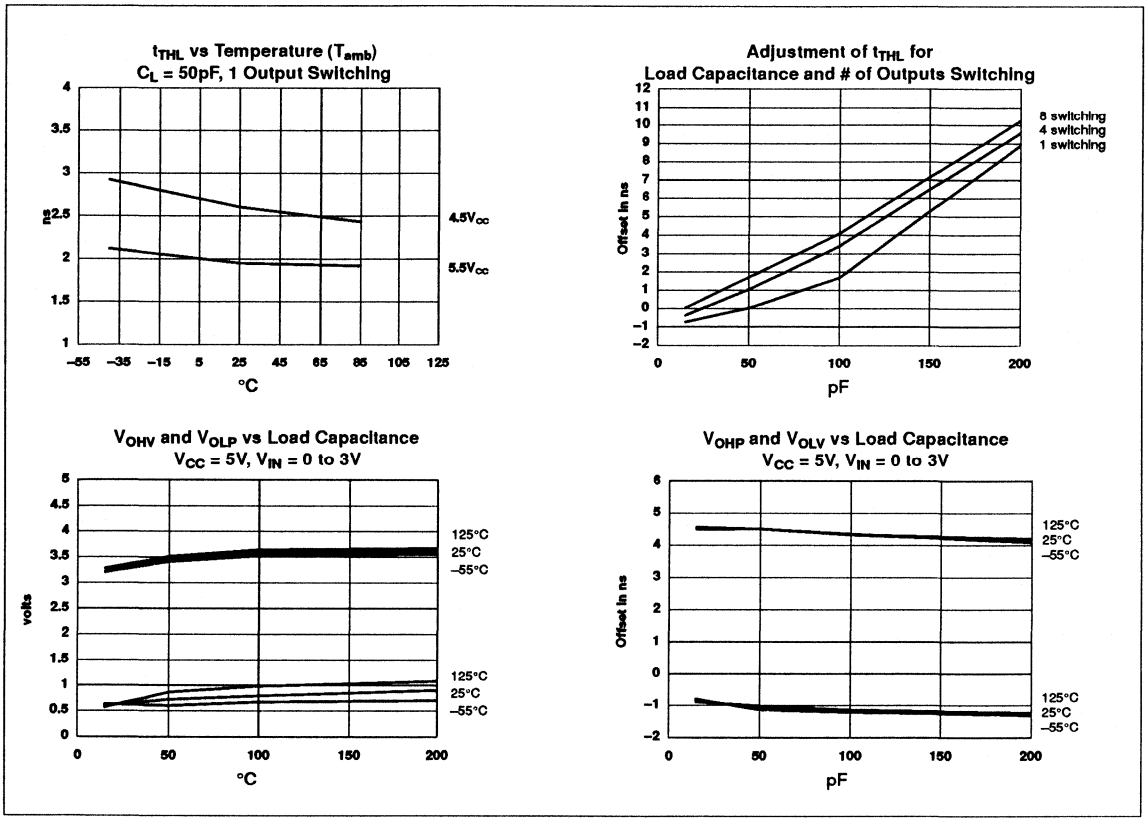


t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching




t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V_{CC}
5.5V_{CC}
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
8 switching
4 switching
1 switching
V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
volts
°C
125°C
25°C
–55°C
V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
Offset in ns
pF
125°C
25°C
–55°C

Transceiver/register, inverting (3-State)

74ABT651

FEATURES

- Independent registers for A and B buses
- The 74ABT651 is the inverting version of the 74ABT652.
- Multiplexed real-time and stored data
- 3-State outputs
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT651 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT651 Transceiver/ Register consists of bus transceiver circuits with 3-State, inverting outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{OEBA}$) and Select (SAB, SBA) pins are provided for bus management.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	C_L = 50pF; V_{CC} = 5V	5.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

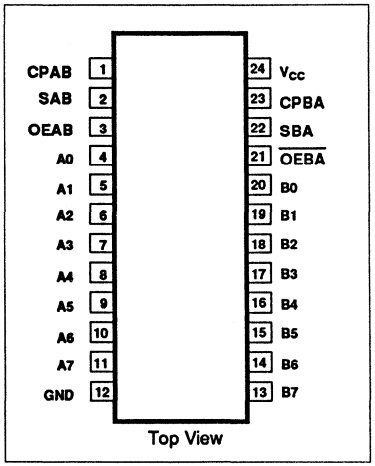
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT651N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT651D

PIN DESCRIPTION

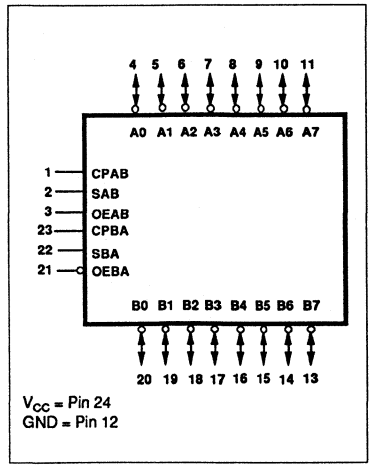
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 23	CPAB / CPBA	Clock input A to B / Clock input B to A
2, 22	SAB / SBA	Select input A to B / Select input B to A
3, 21	OEAB / $\overline{OEBA}$	Output enable inputs
4, 5, 6, 7 8, 9, 10, 11	A0 - A7	Data inputs/outputs (A side)
20, 19, 18, 17 16, 15, 14, 13	B0 - B7	Data inputs/outputs (B side)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

PIN CONFIGURATION



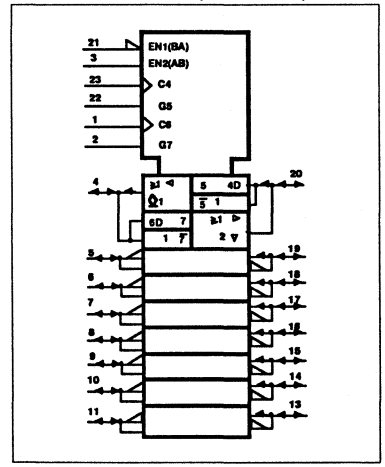
Top View

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS					DATA I/O		OPERATING MODE
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB SBA	An	Bn	
L L	H H	H or L ↑	H or L ↑	X X X X	Input	Input	Isolation Store A and B data
X H	H H	↑ ↑	H or L ↑	X X ** X	Input	Unspecified output *	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X X **	Unspecified output *	Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X L X H	Output	Input	Real time $\overline{B}$ data to A bus Stored $\overline{B}$ data to A bus
H H	H H	X H or L	X X	L X H X	Input	Output	Real time $\overline{A}$ data to B bus Store $\overline{A}$ data to B bus
H	L	H or L	H or L	H H	Output	Output	Stored $\overline{A}$ data to B bus Stored $\overline{B}$ data to A bus

H= High voltage level

L= Low voltage level

*= The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

↑ =Low-to-High clock transition

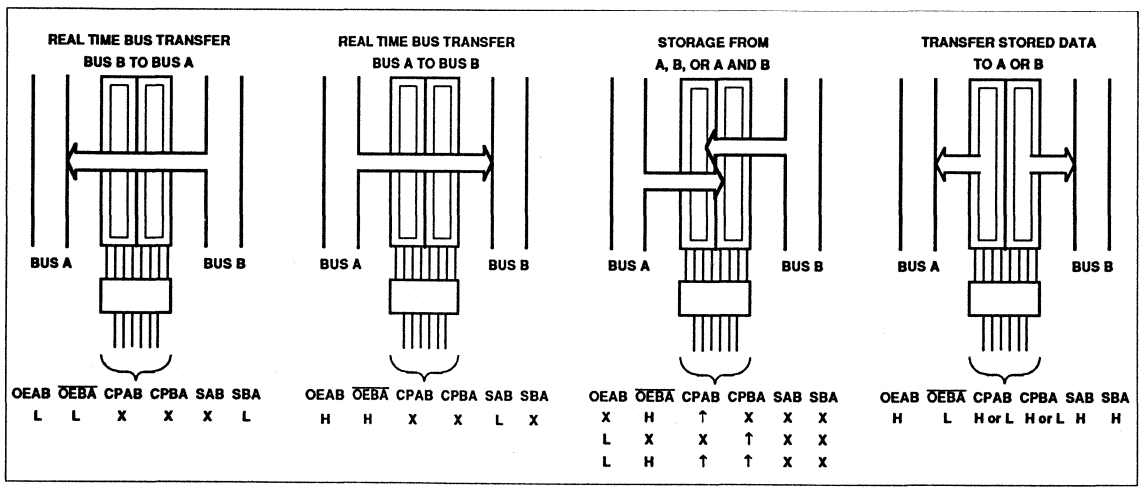
X = Don't care

** If Select control = L, then clocks can occur simultaneously. If Select control = H, the clocks must be staggered in order to load both registers.

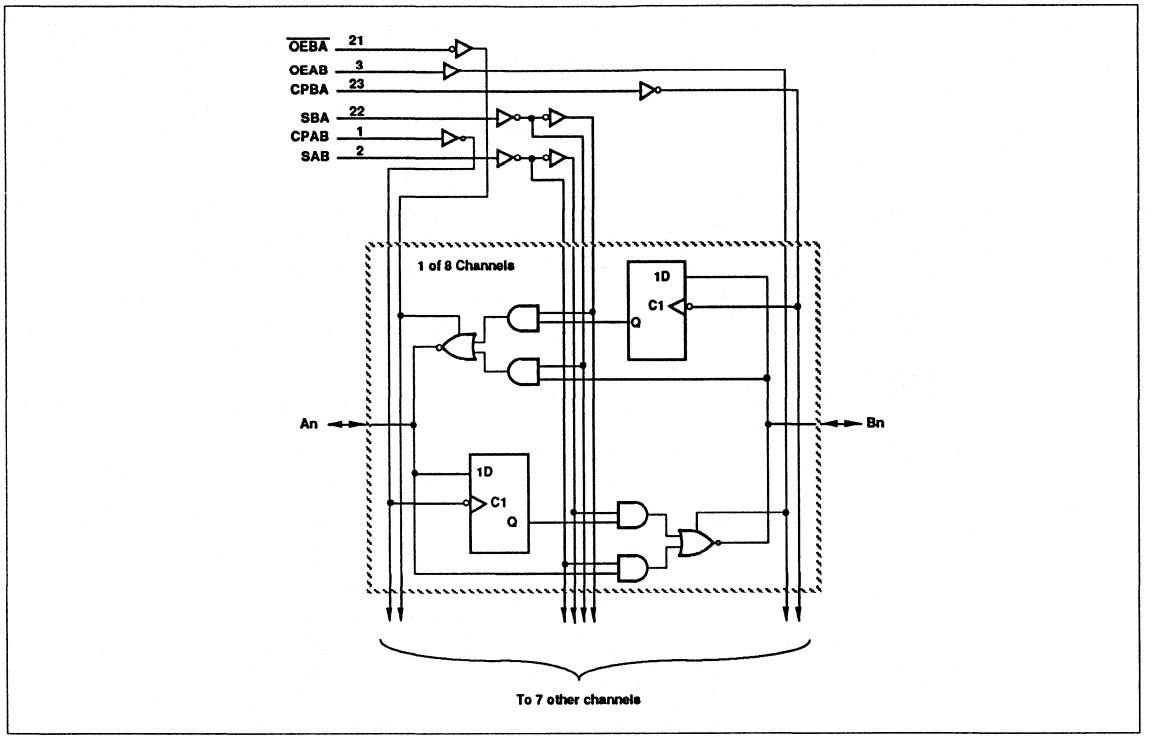
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'ABT651.

The select pins determine whether data is stored or transferred through the device in real time.

The output enable pins determine the direction of the data flow.



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Transceiver/register, non-inverting (3-State) — 74ABT652

FEATURES

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 3-State outputs
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT652 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT652 Transceiver/ Register consists of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{OEBA}$) and Select (SAB, SBA) pins are provided for bus management.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to Anor Bn	C_L = 50pF; V_{CC} = 5V	5.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

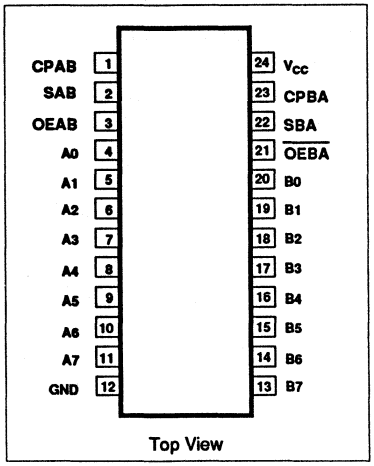
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT652N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT652D

PIN DESCRIPTION

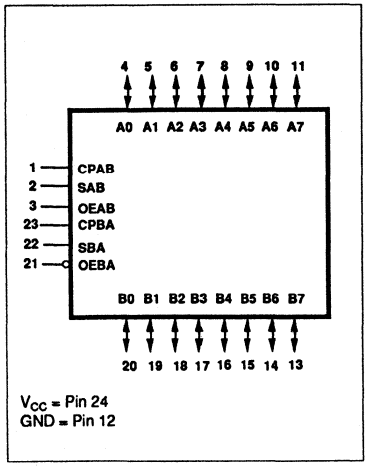
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 23	CPAB / CPBA	Clock input A to B / Clock input B to A
2, 22	SAB / SBA	Select input A to B / Select input B to A
3, 21	OEAB / $\overline{OEBA}$	Output enable inputs
4, 5, 6, 7 8, 9, 10, 11	A0 - A7	Data inputs/outputs (A side)
20, 19, 18, 17 16, 15, 14, 13	B0 - B7	Data inputs/outputs (B side)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

PIN CONFIGURATION



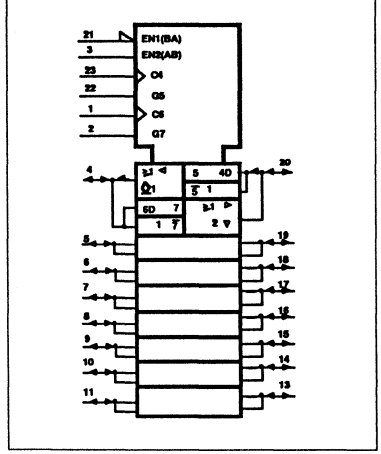
Top View

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)



Transceiver/register, non-inverting (3-State) 74ABT652

FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	An	Bn	
L	H	H or L	H or L	X	X	Input	Input	Isolation Store A and B data
L	H	↑	↑	X	X			
X	H	↑	H or L	X	X	Input	Unspecified output *	Store A, Hold B Store A in both registers
H	H	↑	↑	**	X			
L	X	H or L	↑	X	X	Unspecified output *	Input	Hold A, Store B Store B in both registers
L	L	↑	↑	X	**			
L	L	X	X	X	L	Output	Input	Real time B data to A bus Stored B data to A bus
L	L	X	H or L	X	H			
H	H	X	X	L	X	Input	Output	Real time A data to B bus Store A data to B bus
H	H	H or L	X	H	X			
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus Stored B data to A bus

H = High voltage level

L= Low voltage level

*= The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

↑ =Low-to-High clock transition

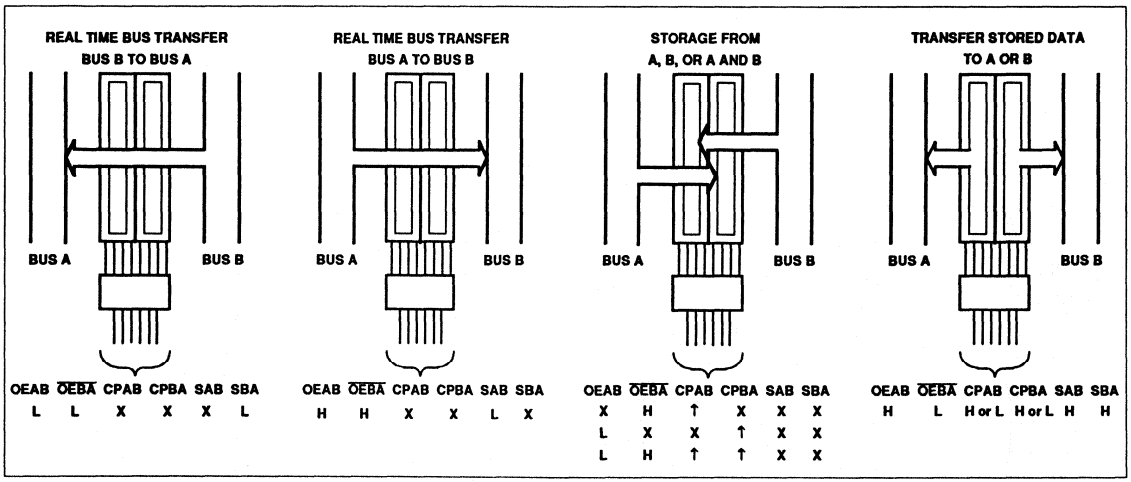
X = Don't care

** If Select control = L, then clocks can occur simultaneously. If Select control = H, the clocks must be staggered in order to load both registers.

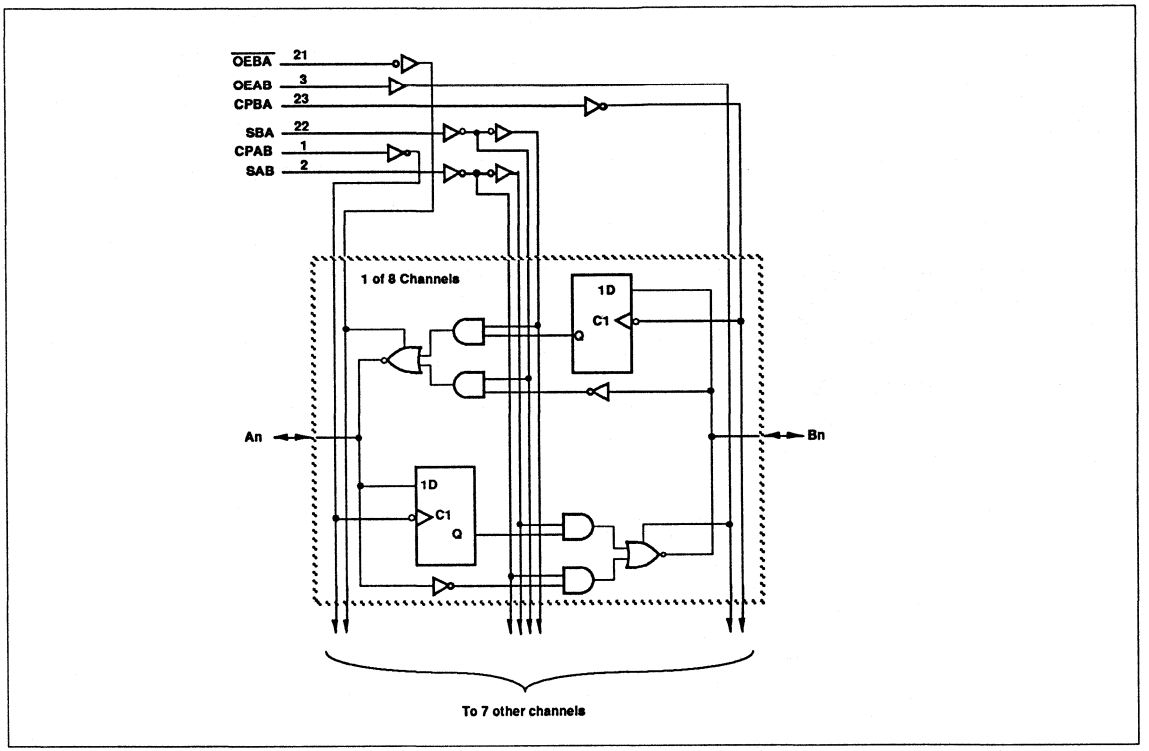
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ABT652.

The select pins determine whether data is stored or transferred through the device in real time.

The output enable pins determine the direction of the data flow.



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Octal transceiver with parity generator/checker (3-State)

74ABT657

FEATURES

- Combinational functions in one package
- Low static and dynamic power dissipation with high speed and high output drive
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT657 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT657 is an octal transceiver featuring non-inverting buffers with 3-State outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 64mA. The Transmit/Receive ($T/\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active-High) enables data from A ports to B ports; Receive (active-Low) enables data from B ports to A ports.

The Output Enable ($\overline{OE}$) input disables both the A and B ports by placing them in a high impedance condition when the $\overline{OE}$ input is High. The parity select (ODD/$\overline{EVEN}$) input gives the user the option of odd or even parity systems. The parity (PARITY) pin is an output from the generator/checker when transmitting from the port A to B ($T/\overline{R}$ = High) and an input when receiving from port B to A port ($T/\overline{R}$ = Low). When transmitting ($T/\overline{R}$ = High) the parity select (ODD/$\overline{EVEN}$) input is set, then the A port data is polled to determine the number of High bits. The parity (PARITY) output then goes to the logic state determined by the parity select (ODD/$\overline{EVEN}$) setting and by the number of High bits on port A. For example, if the parity select (ODD/$\overline{EVEN}$) is set Low (even parity), and the number of High bits on port A is odd, then the parity (PARITY) output will be High, transmitting even parity. If the number of High bits on port A is even, then the parity (PARITY) output will be Low, keeping even parity. When in receive mode ($T/\overline{R}$ = Low) the B port is polled to determine the number of High bits. If parity select (ODD/$\overline{EVEN}$) is Low (even parity) and the number of Highs on port B is:

(1) odd and the parity (PARITY) input is High, then $\overline{ERROR}$ will be High, signifying no error.

(2) even and the parity (PARITY) input is High, then $\overline{ERROR}$ will be asserted Low, indicating an error.

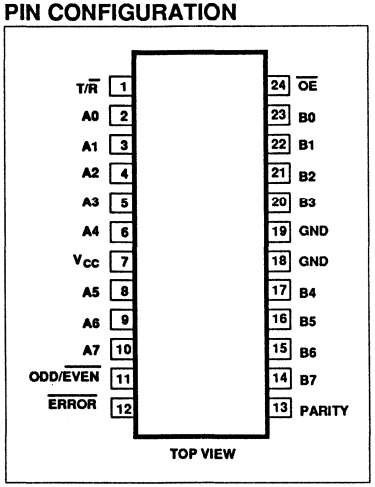
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

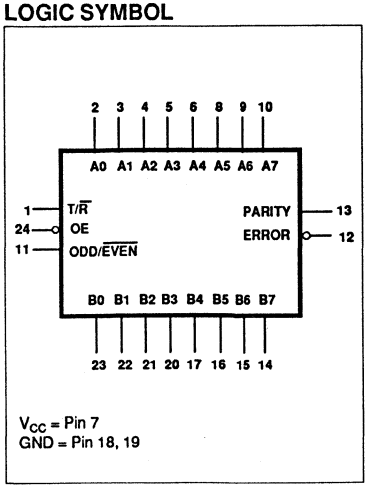
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT657N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT657D

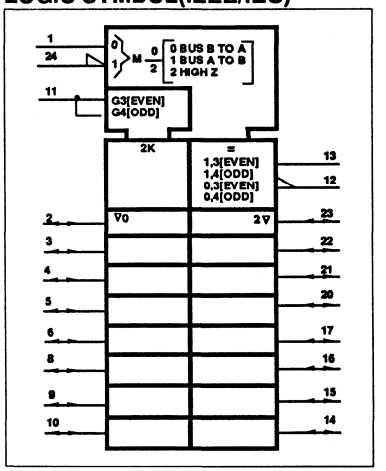
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
13	PARITY	Parity output
11	ODD/EVEN	Parity select input
12	$\overline{\text{ERROR}}$	Error output
1	T/$\overline{\text{R}}$	Transmission/Receive input
2, 3, 4, 5, 6 8, 9, 10	A0 - A7	A port 3-State outputs
23, 22, 21, 20 17, 16, 15, 14	B0 - B7	B port 3-State outputs
24	$\overline{\text{OE}}$	Ouput enable input activelow
18, 19	GND	Ground (0V)
7	V_{CC}	Positive supply voltage

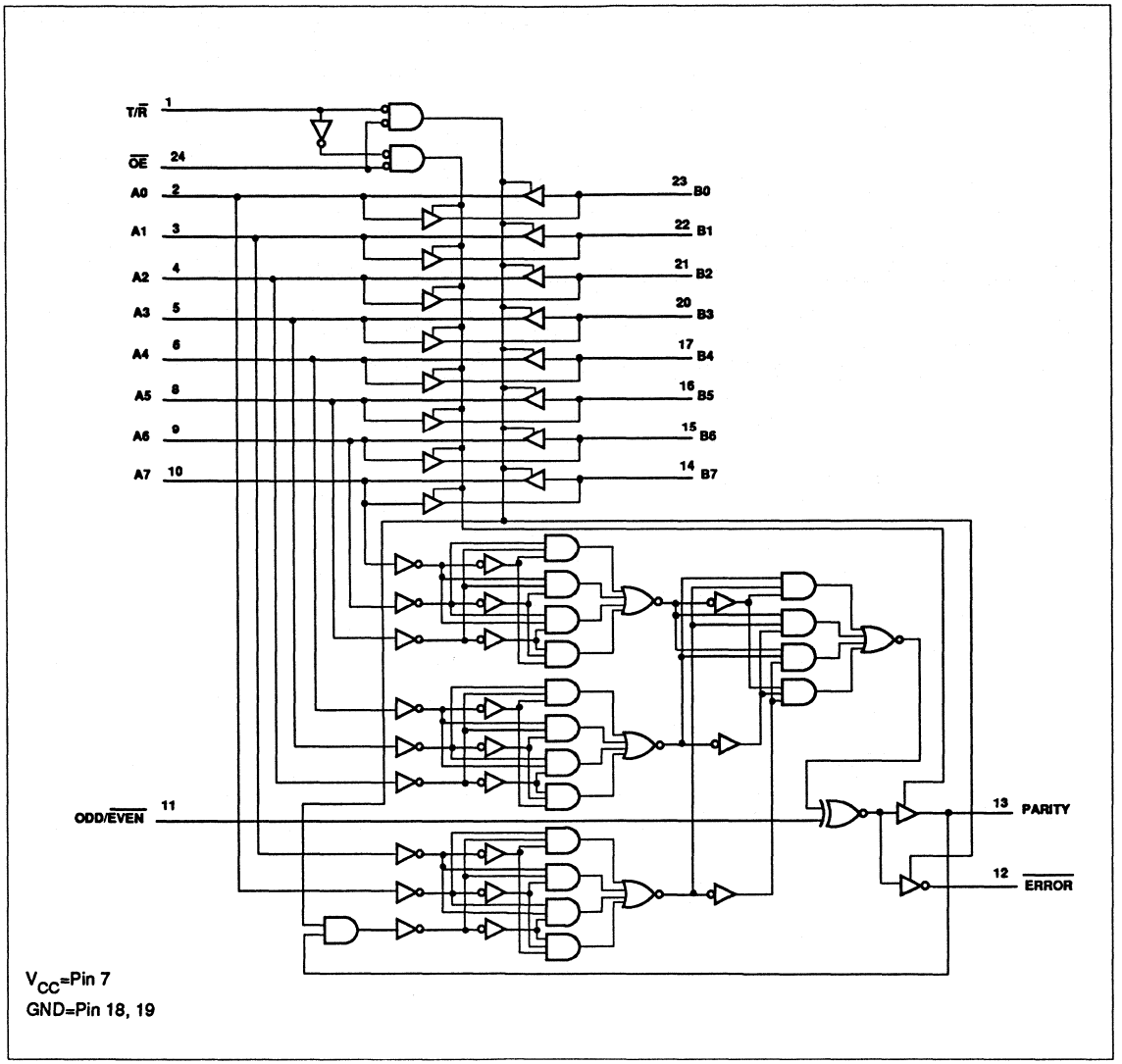
FUNCTION TABLE

NUMBER OF INPUTS THAT ARE HIGH	INPUTS			INPUT/ OUPUT	OUTPUTS	
	$\overline{\text{OE}}$	T/$\overline{\text{R}}$	ODD/$\overline{\text{EVEN}}$	PARITY	$\overline{\text{ERROR}}$	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	3-state

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

Octal transceiver with parity generator/checker (3-State) 74ABT657

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
I_{IH} + I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC ELECTRICAL CHARACTERISTICS

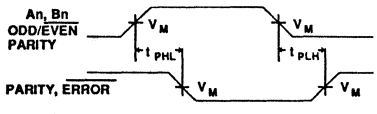
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF. R_L = 500Ω

SYMBOL	PARAMETER	TEST CONDITION	74ABT657					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40° C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 2	1.1 1.2	3.3 3.0	5.0 4.3	1.1 1.2	5.5 4.8	ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	Waveform 1,2	2.6 3.2	6.5 7.0	9.1 9.4	2.6 3.2	11.0 11.3	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{EVEN}$ to PARITY, $\overline{ERROR}$	Waveform 1,2	1.7 1.9	5.0 5.0	6.8 6.7	1.7 1.9	7.7 7.6	ns
t_{PLH} t_{PHL}	Propagation delay Bn to $\overline{ERROR}$	Waveform 1,2	5.3 5.2	9.2 9.6	12.1 12.9	5.3 5.2	15.1 15.7	ns
t_{PLH} t_{PHL}	Propagation delay PARITY to $\overline{ERROR}$	Waveform 1,2	2.8 3.5	6.0 6.4	8.1 8.3	2.8 3.5	10.1 10.2	ns
t_{PZH} t_{PZL}	Output Enable time[1] to High or Low level	Waveform 3 Waveform 4	1.3 1.9	3.8 4.4	5.6 7.0	1.3 1.9	6.7 8.2	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 3 Waveform 4	3.1 3.4	5.1 5.4	7.0 7.6	3.1 3.4	10.5 8.0	ns

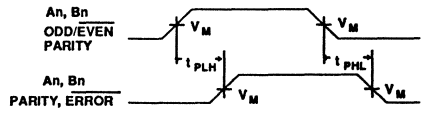
NOTE:

1. These delay times reflect the 3-State recovery time only and do not include the delay through the buffers and the parity check circuitry which affect the $\overline{ERROR}$ output. To assure *VALID* information at the $\overline{ERROR}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{ERROR}$ output. *VALID* data at the $\overline{ERROR}$ pin ≥ (B to A) + (A to PARITY).

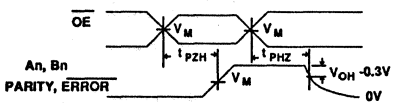
AC WAVEFORMS



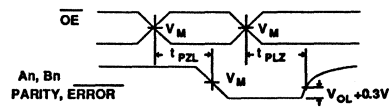
Waveform 1. Propagation Delay for Inverting Outputs



Waveform 2. Propagation Delay for Non-Inverting Outputs



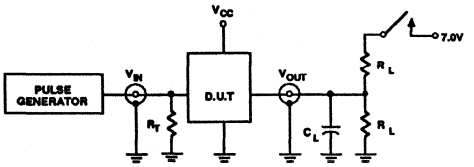
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

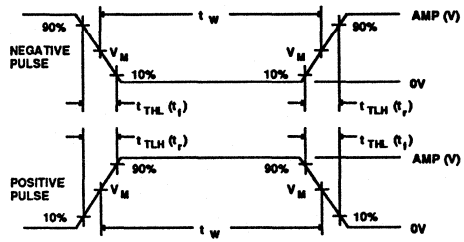
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

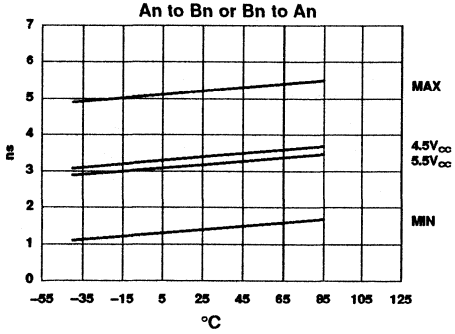


V_M = 1.5V

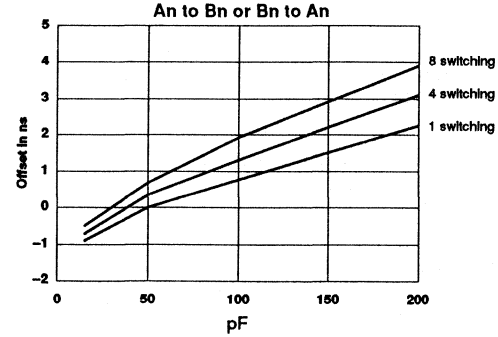
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

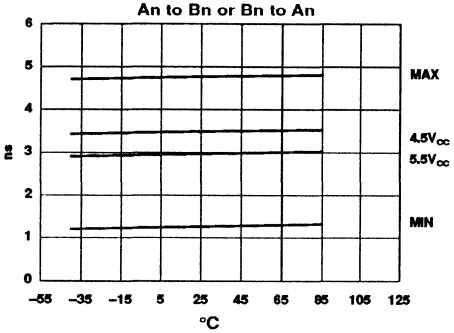
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
An to Bn or Bn to An



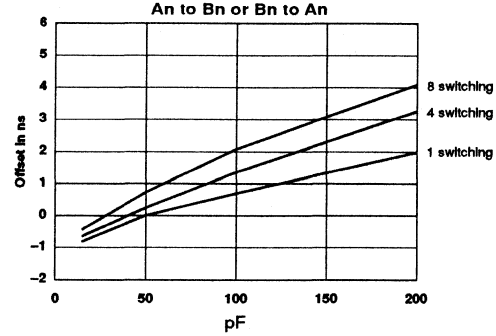
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
An to Bn or Bn to An



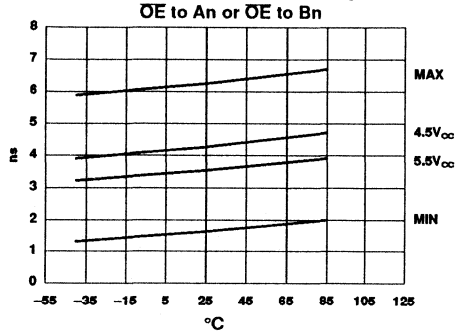
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
An to Bn or Bn to An



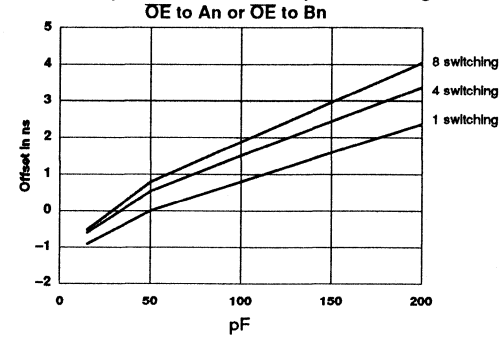
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
An to Bn or Bn to An



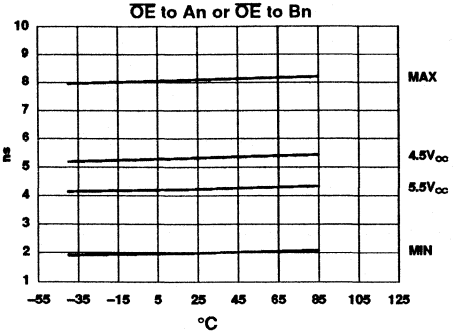
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



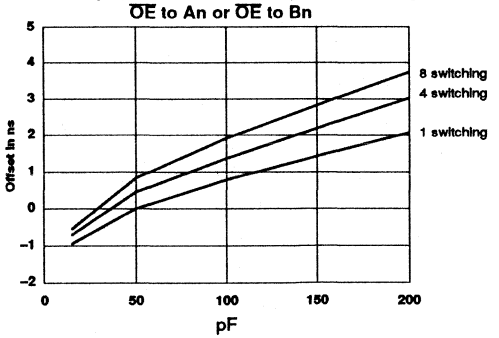
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



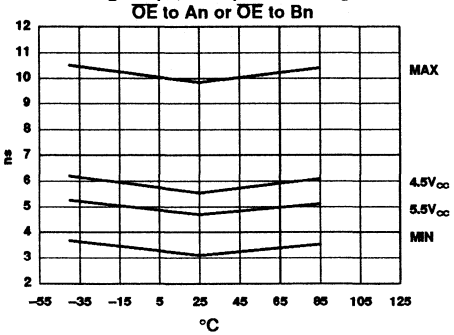
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



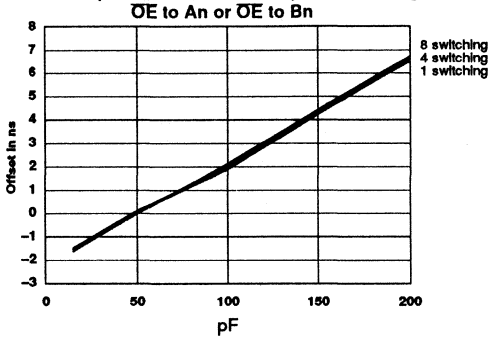
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



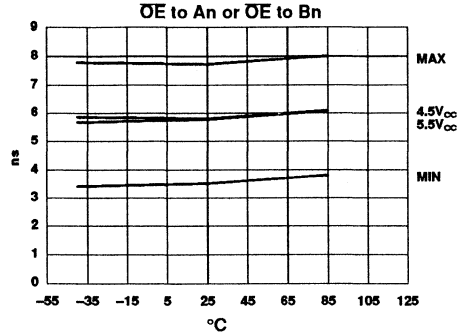
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



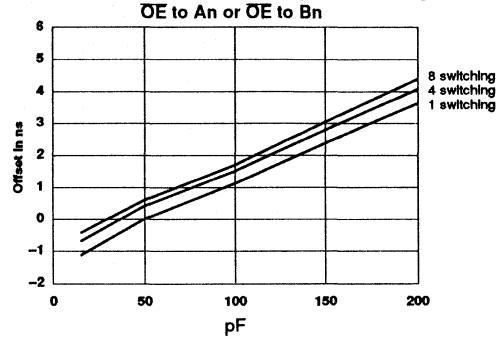
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



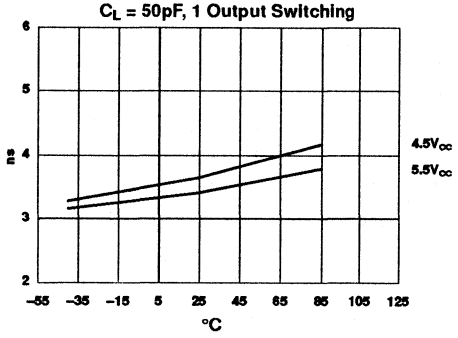
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



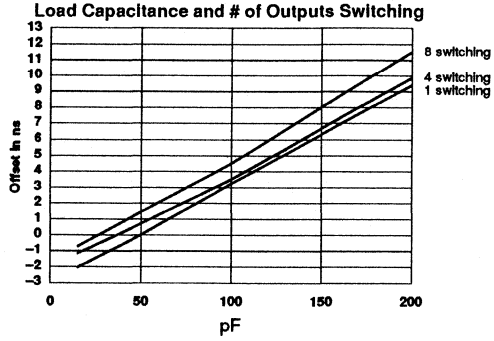
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$\overline{OE}$ to An or $\overline{OE}$ to Bn



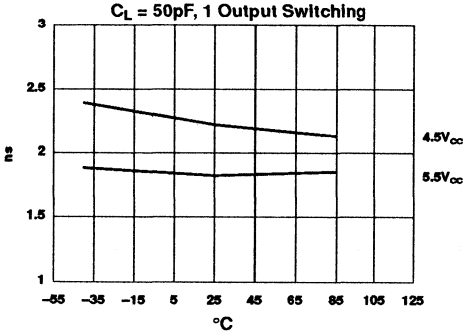
t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



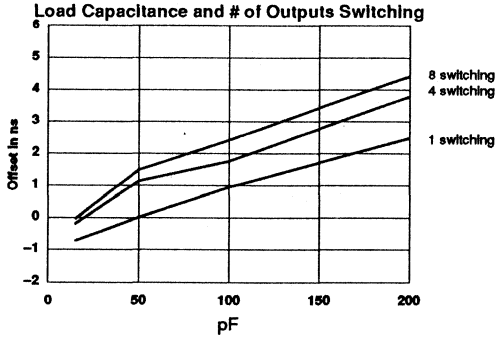
Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching



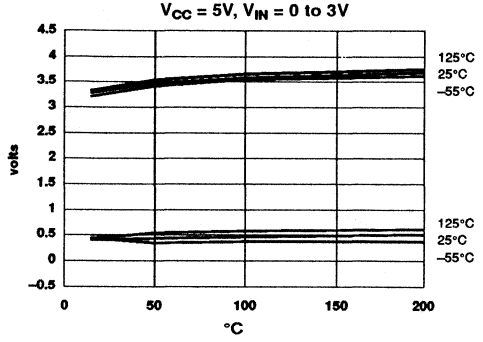
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



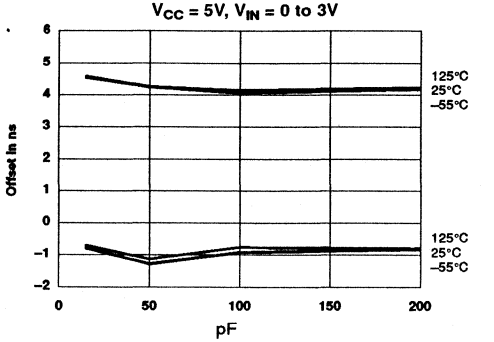
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching



V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



10-bit D-type flip-flop; positive-edge trigger (3-State) — 74ABT821

FEATURES

- High speed parallel registers with positive edge-triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT821 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT821 Bus interface Register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 'ABT821 is a buffered 10-bit wide version of the 'ABT374/'ABT534 functions.

The 'ABT821 is a 10-bit, edge triggered register coupled to ten 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active Low Output Enable ($\overline{OE}$) controls all ten 3-State buffers independent of the register operation. When $\overline{OE}$ is Low, the data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

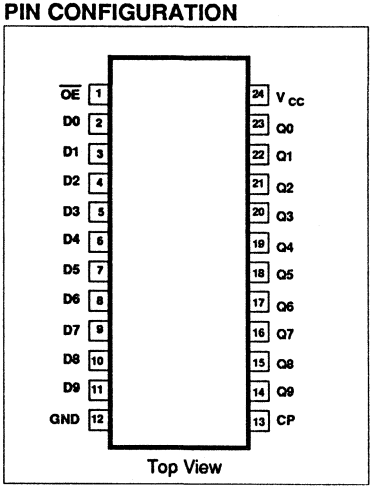
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	5.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

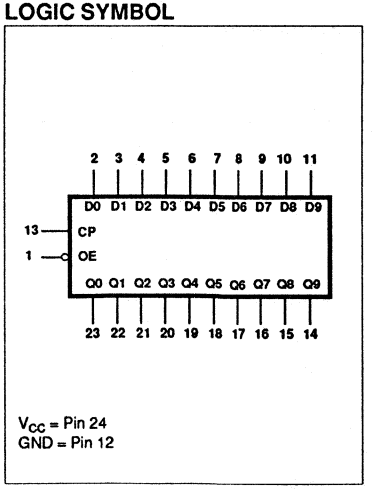
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP	-40°C to +85°C	74ABT821N
24-pin plastic SOL	-40°C to +85°C	74ABT821D

PIN CONFIGURATION



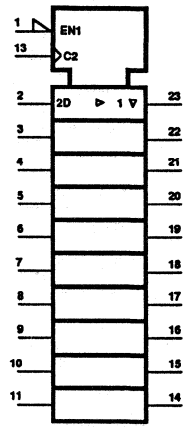
Top View

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)



10-bit D-type flip-flop; positive-edge trigger (3-State) 74ABT821

PIN DESCRIPTION

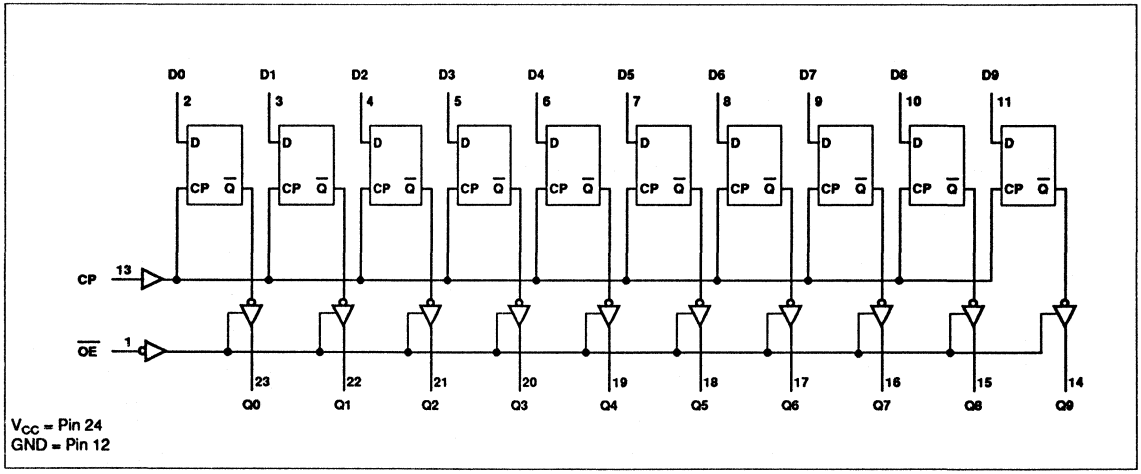
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output Enable input (active Low)
2, 3, 4, 5, 6, 7 8, 9, 10, 11	D0 - D9	Data inputs
14, 15, 16, 17, 18, 19, 20, 21, 22, 23	Q0 - Q9	Data outputs
13	CP	Clock Pulse input (active rising edge)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn	REGISTER	Q0 - Q9	
L L	↑ ↑	l h	L H	L H	Load and read register
L	‡	X	NC	NC	Hold
H H	‡ ↑	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
‡ = Not a Low-to-High clock transition

LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		30	38		38	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

9-bit D-type flip-flop with reset and enable; (3-State) — 74ABT823

FEATURES

- High speed parallel registers with positive edge-triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT823 Bus interface Register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 'ABT823 is a 9-bit wide buffered register with Clock Enable ($\overline{CE}$) and Master Reset ($\overline{MR}$) which are ideal for parity bus interfacing in high microprogrammed systems.

The register is fully edge-triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	5.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

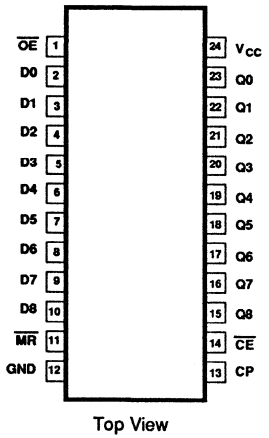
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP	-40°C to +85°C	74ABT823N
24-pin plastic SOL	-40°C to +85°C	74ABT823D

PIN DESCRIPTION

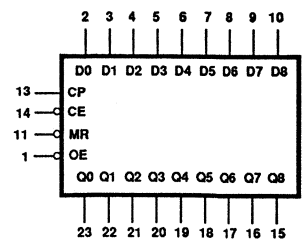
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output Enable input (active Low)
2, 3, 4, 5, 6, 7 8, 9, 10	D0 - D8	Data inputs
15, 16, 17, 18 19, 20, 21, 22, 23	Q0 - Q8	Data outputs
13	CP	Clock Pulse input (active rising edge)
14	$\overline{CE}$	Clock Enable input (active Low)
11	$\overline{MR}$	Master Reset input (active Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

PIN CONFIGURATION



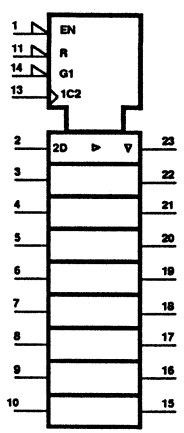
Top View

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)



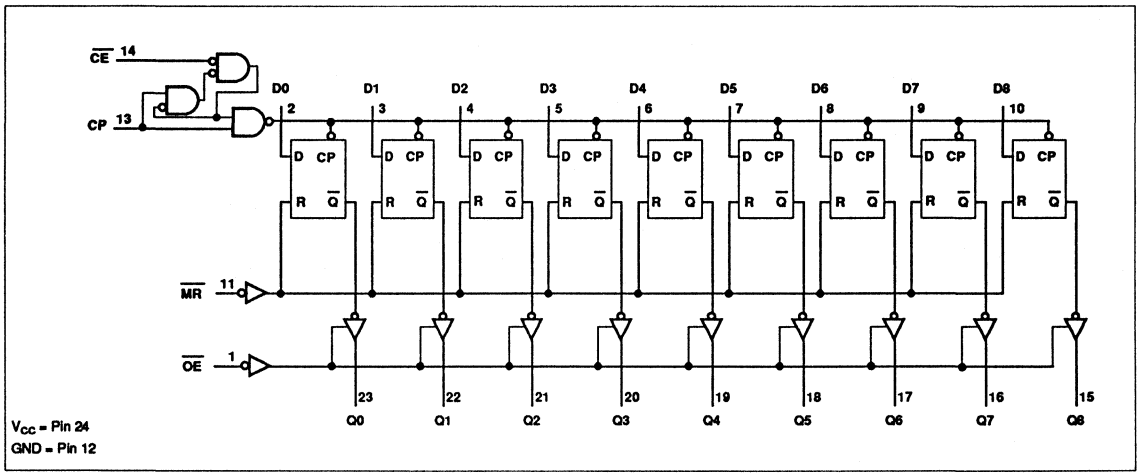
9-bit D-type flip-flop with reset and enable; (3-State) 74ABT823

FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$\overline{OE}$	$\overline{MR}$	$\overline{CE}$	CP	Dn	Q0 - Q8	
L	L	X	X	X	L	Clear
L	H	L	↑	h	H	Load and read data
L	H	L	↑	l	L	
L	H	H	↕	X	NC	Hold
H	X	X	X	X	Z	High impedance

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = Not a Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		27	34		34	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

10-bit buffer/line driver, non-inverting (3-State)

74ABT827

FEATURES

- Ideal where high speed, light bus loading and increased fan-in are required
- Flow through pinout architecture for microprocessor oriented applications
- Outputs capability: +64mA/-32mA
- Slim 300 mil-wide plastic 24-pin package
- Pinout and function compatible with AMD 29827

DESCRIPTION

The 74ABT827 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT827 10-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($\overline{OE0}$, $\overline{OE1}$) for maximum control flexibility.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

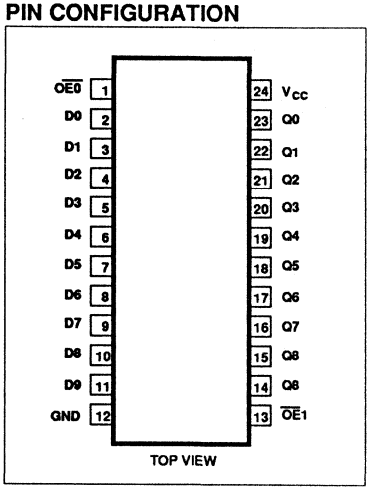
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP	-40°C to +85°C	74ABT827N
24-pin plastic SOL	-40°C to +85°C	74ABT827D

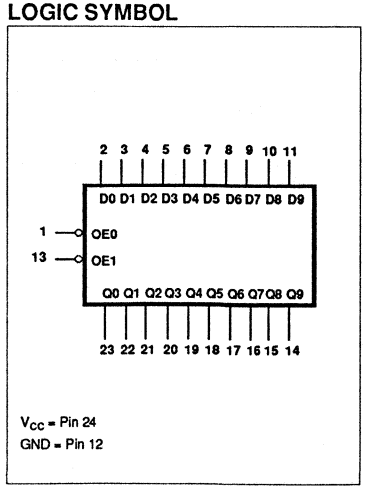
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 13	$\overline{OE0}$ $\overline{OE1}$	Output Enable inputs (active Low)
2, 3, 4, 5, 6, 7 8, 9, 10, 11	D0 - D9	Data inputs
14, 15, 16, 17, 18 19, 20, 21, 22, 23	Q0 - Q9	Data outputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

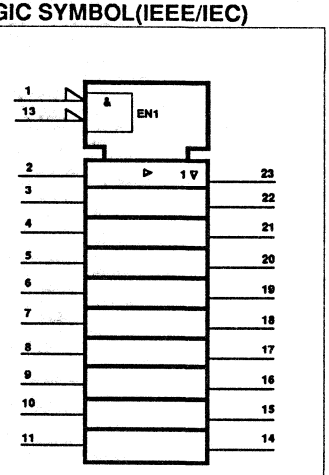
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



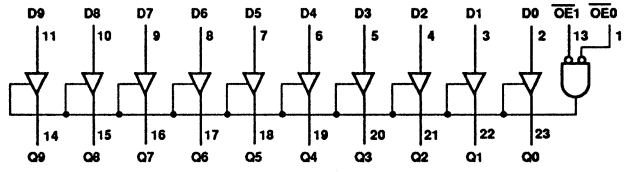
10-bit buffer/line driver, non-inverting (3-State) 74ABT827

FUNCTION TABLE

INPUTS		OUTPUTS	OPERATING MODE
$\overline{OE}_n$	Dn	Qn	
L	L	L	Transparent
L	H	H	Transparent
H	X	Z	High impedance

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		30	38		38	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Octal transceiver with parity generator/checker (3-State)

74ABT833

FEATURES

- Low static and dynamic power dissipation with high speed and high output drive
- Open-collector $\overline{\text{ERROR}}$ output
- Functionally equivalent to AMD AM29833
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT833 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT833 is an octal transceiver with a parity generator/checker and is intended for bus-oriented applications.

When Output Enable A ($\overline{\text{OEA}}$) is High, it will place the A outputs in a high impedance state. Output Enable B ($\overline{\text{OEB}}$) controls the B outputs in the same way.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	2.9	ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	C_L = 50pF; V_{CC} = 5V	6.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

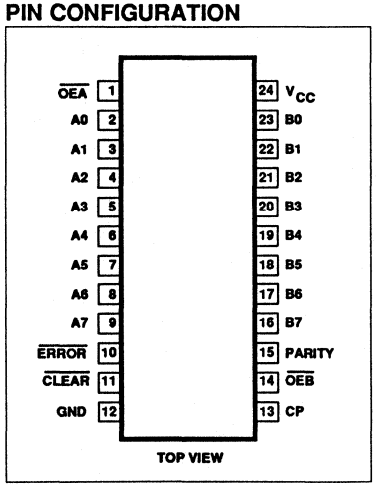
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT833N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT833D

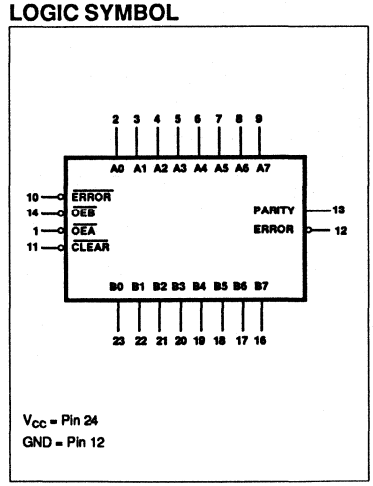
The parity generator creates an odd parity output (PARITY) when $\overline{\text{OEB}}$ is Low. When $\overline{\text{OEA}}$ is low, the parity of the B port, including the PARITY input, is checked for odd parity. When an error is detected, the error data is sent to the input of a storage register. If a Low-to-High transition happens at the clock input (CP), the error data is stored in the register and the Open-collector error flag ($\overline{\text{ERROR}}$) will go Low. The error flag register is cleared with a Low pulse on the $\overline{\text{CLEAR}}$ input.

If both $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ are Low, data will flow from the A bus to the B bus and the part is forced into an error condition which creates an inverted PARITY output. This error condition can be used by the designer for system diagnostics.

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
A0 - A7	2, 3, 4, 5, 6, 7, 8, 9	A port 3-State inputs/outputs
B0 - B7	23, 22, 21, 20, 19, 18, 17, 16	B port 3-State inputs/outputs
$\overline{OEA}$	1	Enables the A outputs when Low
$\overline{OEB}$	14	Enables the B outputs when Low
PARITY	15	Parity output
$\overline{ERROR}$	10	Error output
$\overline{CLEAR}$	11	Clears the error flag register when Low
CP	13	Clock input
GND	12	Ground (0V)
V_{CC}	24	Positive supply voltage

FUNCTION TABLE

MODE	INPUTS						OUTPUT AND I/O			
	$\overline{OEB}$	$\overline{OEA}$	$\overline{CLEAR}$	CP	An Σ of Highs	Bn† Σ of Highs	A	B	PARITY	$\overline{ERROR}$‡
A data to B bus and generate parity	L	H	X	X	Odd Even	NA	NA	A	L H	NA
B data to A bus and check parity	H	L	H	↑	NA	Odd Even	B	NA	NA	H L
Clear error flag register	X	X	L	X	X	X	X	NA	NA	H
A bus and B bus disabled§	H	H	H L H H	‡ ‡ ↑ ↑	X X Odd Even	X	Z	Z	Z	NC H H L
A data to B bus and generate inverted parity (Forced-error)	L	L	X	X	Odd Even	NA	NA	A	H L	NA

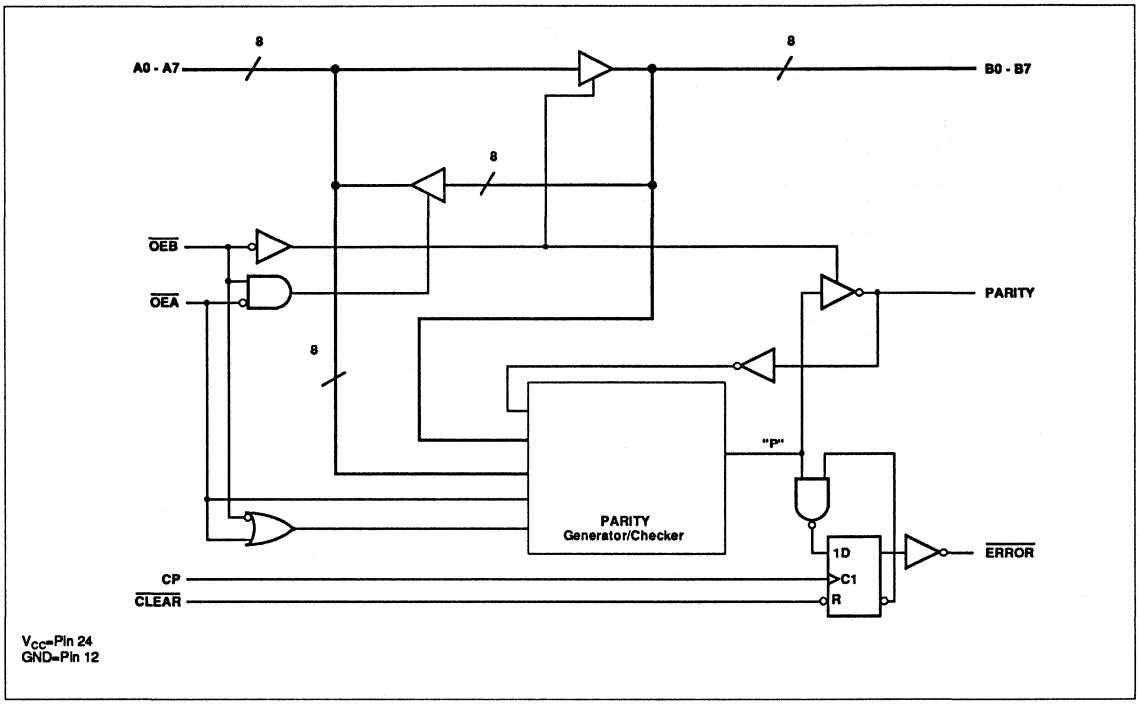
ERROR FLAG FUNCTION TABLE

MODE	INPUTS		Internal node Point "P"	Output Pre-state $\overline{ERROR}_{n-1}$	OUTPUT
	$\overline{CLEAR}$	CP			$\overline{ERROR}$
Sample	H H H	↑ ↑ ↑	H X L	H L X	H L L
Clear	L	X	X	X	H

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care
NA = Not applicable
NC = No change
Z = High-impedance "OFF" state
† = Summation of High-level inputs includes PARITY along with Bn inputs
‡ = Output states shown assume the $\overline{ERROR}$ output was previously High
§ In this mode, the ERROR output, when clocked, shows inverted parity of the A bus
↑ = Low-to-High clock transition
‡ = Not a Low-to-High clock transition

Octal transceiver with parity generator/checker (3-State) 74ABT833

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-.09	-1.2		-1.2	V
I_{OH}	High-level output current $\overline{\text{ERROR}}$ only		V_{CC} = 4.5V; V_{OH} = 4.5V; V_I = V_{IL} or V_{IH}			20		20	µA
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Octal inverting transceiver with parity generator/checker (3-State)

74ABT834

FEATURES

- Low static and dynamic power dissipation with high speed and high output drive
- Open-collector $\overline{\text{ERROR}}$ output
- Functionally equivalent to AMD AM29834
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT834 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT834 is an octal inverting transceiver with a parity generator/checker and is intended for bus-oriented applications.

When Output Enable A ($\overline{\text{OEA}}$) is High, it will place the A outputs in a high impedance state. Output Enable B ($\overline{\text{OEB}}$) controls the B outputs in the same way.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Anto Bn or Bnto An	C_L = 50pF; V_{CC} = 5V	2.9	ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	C_L = 50pF; V_{CC} = 5V	6.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

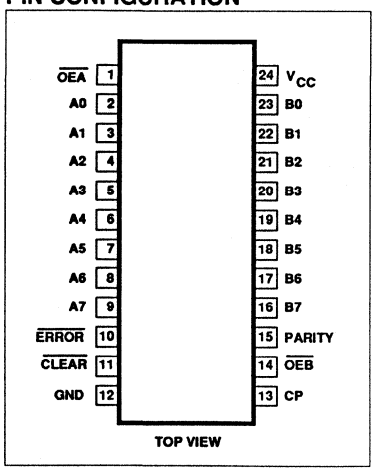
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT834N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT834D

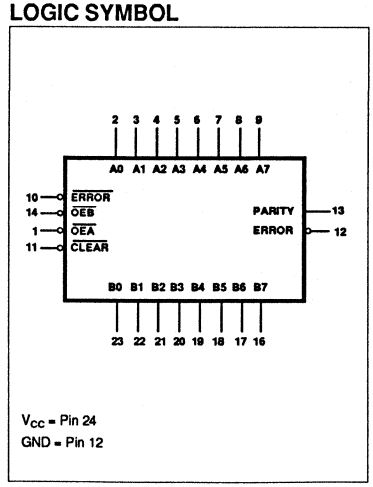
The parity generator creates an odd parity output (PARITY) when $\overline{\text{OEB}}$ is Low. When $\overline{\text{OEA}}$ is low, the parity of the B port, including the PARITY input, is checked for odd parity. When an error is detected, the error data is sent to the input of a storage register. If a Low-to-High transition happens at the clock input (CP), the error data is stored in the register and the Open-collector error flag ($\overline{\text{ERROR}}$) will go Low. The error flag register is cleared with a Low pulse on the $\overline{\text{CLEAR}}$ input.

If both $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ are Low, data will flow from the A bus to the B bus and the part is forced into an error condition which creates an inverted PARITY output. This error condition can be used by the designer for system diagnostics.

PIN CONFIGURATION



LOGIC SYMBOL



Octal inverting transceiver with parity generator/checker (3-State)

74ABT834

PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
A0 - A7	2, 3, 4, 5, 6, 7, 8, 9	A port 3-State inputs/outputs
B0 - B7	23, 22, 21, 20, 19, 18, 17, 16	B port 3-State inputs/outputs
$\overline{OEA}$	1	Enables the A outputs when Low
$\overline{OEB}$	14	Enables the B outputs when Low
PARITY	15	Parity output
$\overline{ERROR}$	10	Error output
$\overline{CLEAR}$	11	Clears the error flag register when Low
CP	13	Clock input
GND	12	Ground (0V)
V_{CC}	24	Positive supply voltage

FUNCTION TABLE

MODE	INPUTS						OUTPUT AND I/O			
	$\overline{OEB}$	$\overline{OEA}$	$\overline{CLEAR}$	CP	An Σ of Highs	Bn† Σ of Highs	A	B	PARITY	$\overline{ERROR}$‡
A data to B bus and generate parity	L	H	X	X	Odd Even	NA	NA	$\overline{A}$	L H	NA
B data to A bus and check parity	H	L	H	↑	NA	Odd Even	$\overline{B}$	NA	NA	H L
Clear error flag register	X	X	L	X	X	X	X	NA	NA	H
A bus and B bus disabled§	H	H	H L H H	‡ ‡ ↑ ↑	X X Odd Even	X	Z	Z	Z	NC H H L
A data to B bus and generate inverted parity (Forced-error)	L	L	X	X	Odd Even	NA	NA	$\overline{A}$	H L	NA

ERROR FLAG FUNCTION TABLE

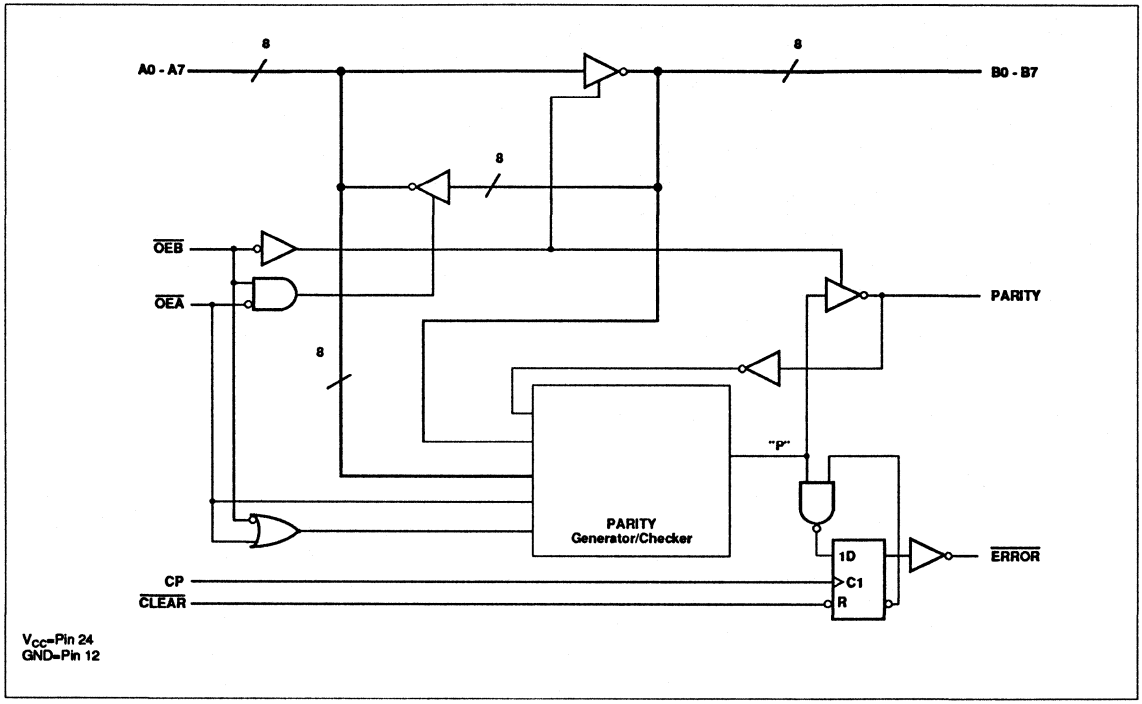
MODE	INPUTS		Internal node Point "P"	Output Pre-state $\overline{ERROR}_{n-1}$	OUTPUT
	$\overline{CLEAR}$	CP			$\overline{ERROR}$
Sample	H H H	↑ ↑ ↑	H X L	H L X	H L L
Clear	L	X	X	X	H

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care
NA = Not applicable
NC = No change
Z = High-impedance "OFF" state
† = Summation of High-level inputs includes PARITY along with Bn inputs
‡ = Output states shown assume the $\overline{ERROR}$ output was previously High
§ In this mode, the ERROR output, when clocked, shows inverted parity of the A bus
↑ = Low-to-High clock transition
‡ = Not a Low-to-High clock transition

Octal inverting transceiver with parity generator/checker (3-State)

74ABT834

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-.09	-1.2		-1.2	V
I_{OH}	High-level output current $\overline{ERROR}$ only		V_{CC} = 4.5V; V_{OH} = 4.5V; V_I = V_{IL} or V_{IH}			20		20	µA
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

10-bit bus interface latch (3-State)

74ABT841

FEATURES

- High speed parallel latches
- Extra data width for wide address/ data paths or buses carrying parity
- Ideal where high speed, light loading, or increased fan-in are required as with MOS microprocessors
- Output capability: +64mA/-32mA
- Slim Dip 300 mil package
- Broadside pinout
- Pin-for-pin and function compatible with AMD AM29841

DESCRIPTION

The 74ABT841 bus interface latch is designed to provide extra data width for wider address/data paths of buses carrying parity.

The 74ABT841 is functionally, and pin compatible to the AMD AM29841.

The 74ABT841 consists of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the LE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output Enable ($\overline{OE}$) is Low. When $\overline{OE}$ is High the output is in the High-impedance state.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50pF; V_{CC} = 5V	4.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

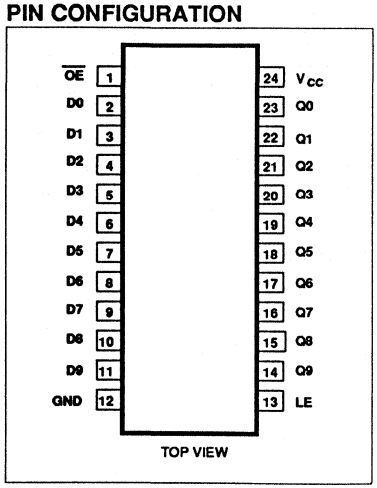
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP	-40°C to +85°C	74ABT841N
24-pin plastic SOL	-40°C to +85°C	74ABT841D

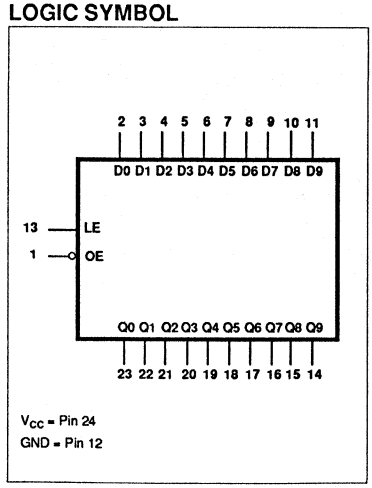
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output Enable input (active Low)
2, 3, 4, 5, 6, 7 8, 9, 10, 11	D0 - D9	Data inputs
14, 15, 16, 17, 18 19, 20, 21, 22, 23	Q0 - Q9	Data outputs
13	LE	Latch Enable input (active falling edge)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

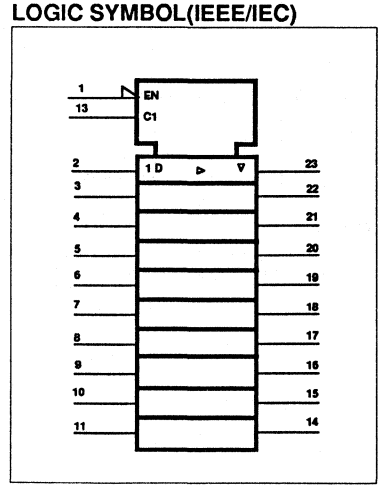
PIN CONFIGURATION



LOGIC SYMBOL

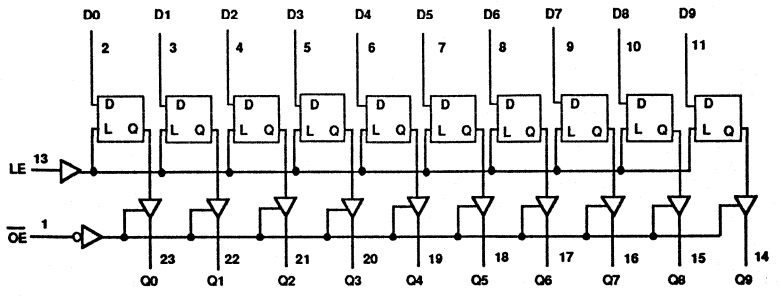


LOGIC SYMBOL(IEEE/IEC)



10-bit bus interface latch (3-State) 74ABT841

LOGIC DIAGRAM



V_{CC} = Pin 24

GND = Pin 12

FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{OE}$	LE	Dn	Qn	
L	H	L	L	Transparent
L	H	H	H	
L	↓	l	L	Latched
L	↓	h	H	
H	X	X	Z	High impedance
L	L	X	NC	Hold

H= High voltage level
L= Low voltage level
h= High state one setup time before the High-to-Low LE transition
l = Low state one setup time before the High-to-Low LE transition
↓= High-to-Low transition
X=Don't care
NC=No change
Z =High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		30	38		38	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

9-bit bus interface latch with set and reset (3-State) — 74ABT843

FEATURES

- High speed parallel latches
- Extra data width for wide address/ data paths or buses carrying parity
- Ideal where high speed, light loading, or increased fan-in are required as with MOS microprocessors
- Output capability: +64mA/-32mA
- Slim Dip 300 mil package
- Broadside pinout
- Pin-for-pin and function compatible with AMD AM29843

DESCRIPTION

The 'ABT843 consists of nine D-type latches with 3-State outputs. In addition to the LE and $\overline{OE}$ pins, the 'ABT843 has a Master Reset ($\overline{MR}$) pin and Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{MR}$ is Low, the outputs are Low if $\overline{OE}$ is Low. When $\overline{MR}$ is High, data can be entered into the latch. When $\overline{PRE}$ is Low, the outputs are High, if $\overline{OE}$ is Low. $\overline{PRE}$ overrides $\overline{MR}$.

The 'ABT843 is functionally, and pin compatible to the AMD AM29843.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_A = 25°C$; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	$C_L = 50pF$; $V_{CC} = 5V$	4.0	ns
C_{IN}	Input capacitance	$V_I = 0V$ or V_{CC}	4	pF
C_{OUT}	Output capacitance	$V_I = 0V$ or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; $V_{CC} = 5.5V$	500	nA

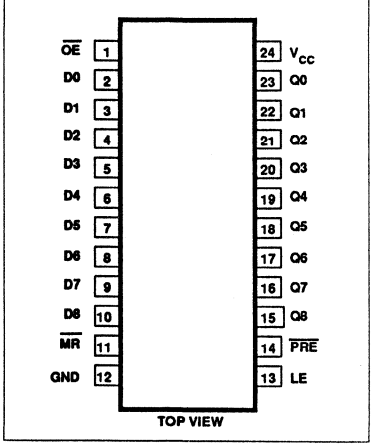
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP	-40°C to +85°C	74ABT843N
24-pin plastic SOL	-40°C to +85°C	74ABT843D

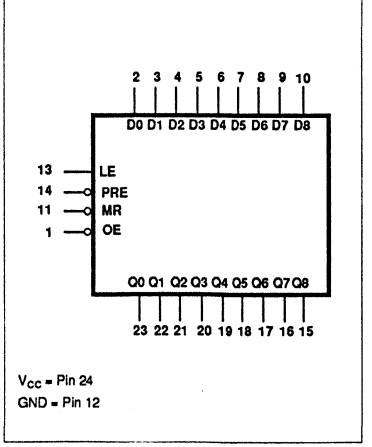
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output Enable input (active Low)
2, 3, 4, 5, 6 7, 8, 9, 10	D0 - D8	Data inputs
15, 16, 17, 18, 19 20, 21, 22, 23	Q0 - Q8	Data outputs
11	$\overline{MR}$	Master Reset input (active Low)
13	LE	Latch Enable input (active falling edge)
14	$\overline{PRE}$	Preset input (active Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

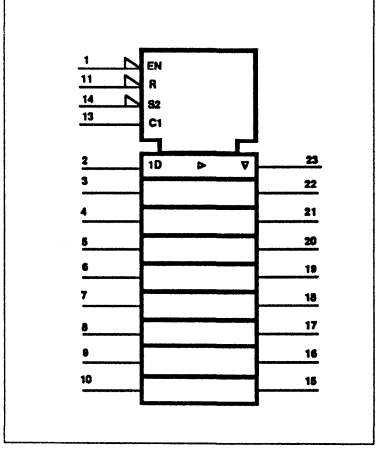
PIN CONFIGURATION



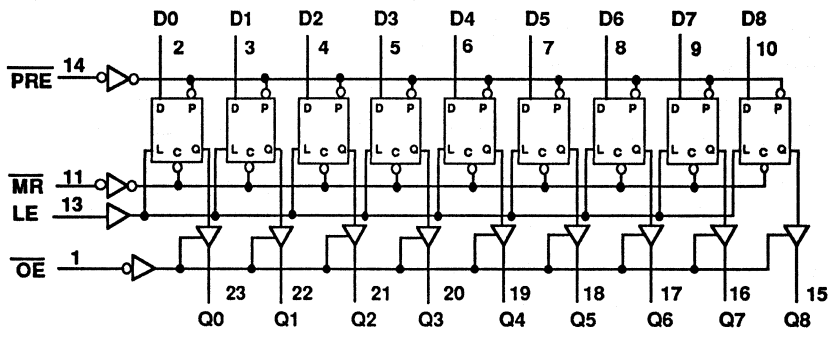
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 24

GND = Pin 12

FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$\overline{OE}$	$\overline{PRE}$	$\overline{MR}$	LE	Dn	Qn	
L	L	X	X	X	H	Preset
L	H	L	X	X	L	Clear
L	H	H	H	L	L	Transparent
L	H	H	H	H	H	
L	H	H	↓	l	L	Latched
L	H	H	↓	h	H	
H	X	X	X	X	Z	High impedance
L	H	H	L	X	NC	Hold

H= High voltage level
L= Low voltage level
h= High state one setup time before the High-to-Low LE transition
l =Low state one setup time before the High-to-Low LE transition
↓=High-to-Low transition
X=Don't care
NC=No change
Z =High impedance "off " state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
I_{IH} + I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		28	34		34	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

8-bit bus interface latch with set and reset (3-State) — 74ABT845

FEATURES

- High speed parallel latches
- Extra data width for wide address/ data paths or buses carrying parity
- Ideal where high speed, light loading, or increased fan-in are required as with MOS microprocessors
- Output capability: +64mA/-32mA
- Slim Dip 300 mil package
- Broadside pinout
- Pin-for-pin and function compatible with AMD AM29845

DESCRIPTION

The 'ABT845 consists of eight D-type latches with 3-state outputs. In addition to the LE, $\overline{OE}$, $\overline{MR}$ and $\overline{PRE}$ pins, the 'ABT845 has two additional $\overline{OE}$ pins making a total of three Output Enables ($\overline{OE}0$, $\overline{OE}1$, $\overline{OE}2$) pins. The multiple Output Enables ($\overline{OE}0$, $\overline{OE}1$, $\overline{OE}2$) allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$.

The 'ABT845 is functionally, and pin compatible to the AMD AM29845.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_A = 25°C$; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	$C_L = 50pF$; $V_{CC} = 5V$	4.0	ns
C_{IN}	Input capacitance	$V_I = 0V$ or V_{CC}	4	pF
C_{OUT}	Output capacitance	$V_I = 0V$ or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; $V_{CC} = 5.5V$	500	nA

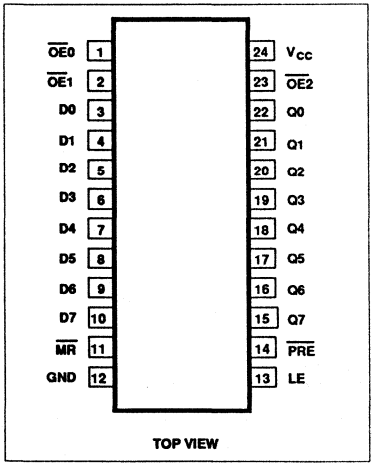
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP	-40°C to +85°C	74ABT845N
24-pin plastic SOL	-40°C to +85°C	74ABT845D

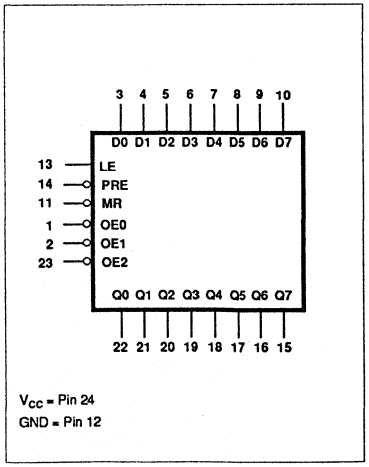
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 23	$\overline{OE}0$ - $\overline{OE}2$	Output Enable input (active Low)
3, 4, 5, 6 7, 8, 9, 10	D0 - D7	Data inputs
15, 16, 17, 18 19, 20, 21, 22	Q0 - Q7	Data outputs
11	$\overline{MR}$	Master Reset input (active Low)
13	LE	Latch Enable input (active falling edge)
14	$\overline{PRE}$	Preset input (active Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

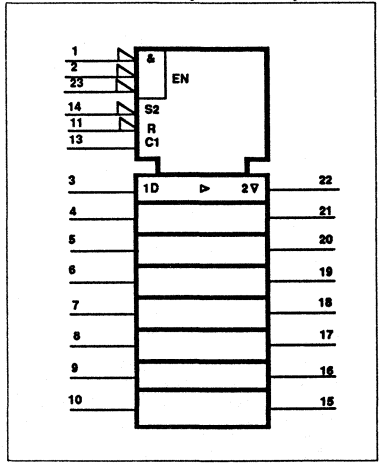
PIN CONFIGURATION



LOGIC SYMBOL

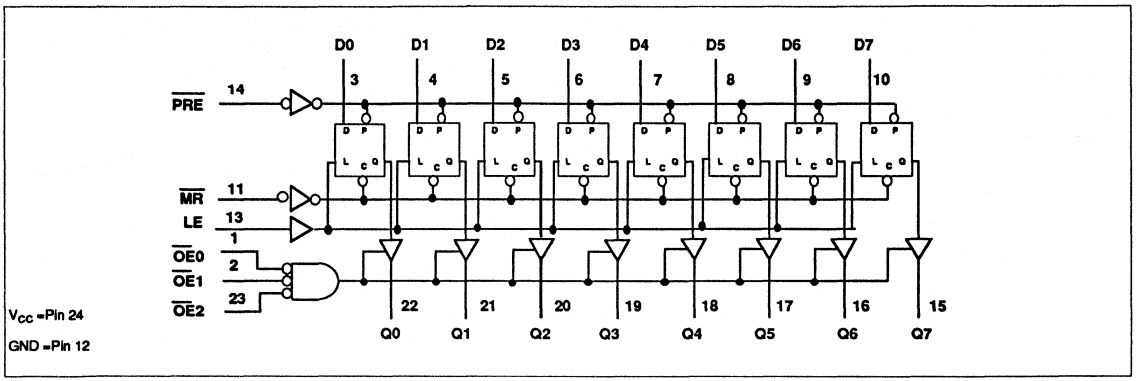


LOGIC SYMBOL (IEEE/IEC)



8-bit bus interface latch with set and reset (3-State) 74ABT845

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$\overline{OE}n$	$\overline{PRE}$	$\overline{MR}$	LE	Dn	Qn	
L	L	X	X	X	H	Preset
L	H	L	X	X	L	Clear
L	H	H	H	L	L	Transparent
L	H	H	H	H	H	
L	H	H	↓	l	L	Latched
L	H	H	↓	h	H	
H	X	X	X	X	Z	High impedance
L	H	H	L	X	NC	Hold

H= High voltage level
L= Low voltage level
h= High state one setup time before the High-to-Low LE transition
l =Low state one setup time before the High-to-Low LE transition
↓=High-to-Low transition
X=Don't care
NC=No change
Z =High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

8-bit transceiver with 9-bit parity checker/ generator and flag latch (3-State)

74ABT853

FEATURES

- Low static and dynamic power dissipation with high speed and high output drive
- Open-collector $\overline{\text{ERROR}}$ output
- Functionally equivalent to AMD AM29853
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT853 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT853 is an octal transceiver with a parity generator/checker and is intended for bus-oriented applications.

When Output Enable A ($\overline{\text{OEA}}$) is High, it will place the A outputs in a high impedance state. Output Enable B ($\overline{\text{OEB}}$) controls the B outputs in the same way.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	2.9	ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	C_L = 50pF; V_{CC} = 5V	6.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

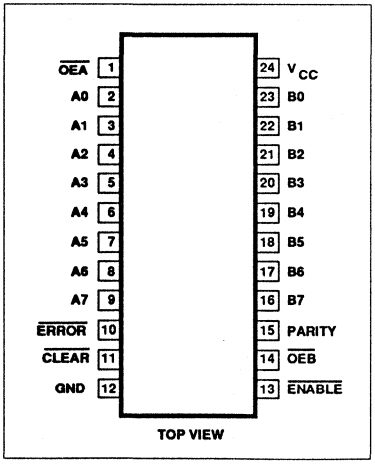
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT853N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT853D

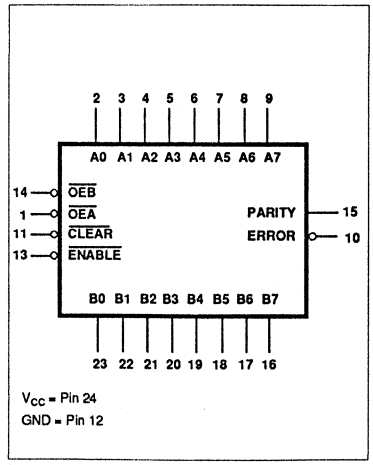
The parity generator creates an odd parity output (PARITY) when $\overline{\text{OEB}}$ is Low. When $\overline{\text{OEA}}$ is Low, the parity of the B port, including the PARITY input, is checked for odd parity. When an error is detected, the error data is sent to the input of a latch. The error data can then be passed, stored, cleared, or sampled depending on the $\overline{\text{ENABLE}}$ and $\overline{\text{CLEAR}}$ control signals.

If both $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ are Low, data will flow from the A bus to the B bus and the part is forced into an error condition which creates an inverted PARITY output. This error condition can be used by the designer for system diagnostics.

PIN CONFIGURATION



LOGIC SYMBOL



8-bit transceiver with 9-bit parity checker/generator and flag latch (3-State)

74ABT853

PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
A0 - A7	2, 3, 4, 5, 6, 7, 8, 9	A port 3-State inputs/outputs
B0 - B7	23, 22, 21, 20, 19, 18, 17, 16	B port 3-State inputs/outputs
$\overline{OEA}$	1	Enables the A outputs when Low
$\overline{OEB}$	14	Enables the B outputs when Low
PARITY	15	Parity output
$\overline{ERROR}$	10	Error output
$\overline{CLEAR}$	11	Clears the error flag register when Low
$\overline{ENABLE}$	13	Enable input (active low)
GND	12	Ground (0V)
V_{CC}	24	Positive supply voltage

FUNCTION TABLE

MODE	INPUTS						OUTPUT AND I/O			
	$\overline{OEB}$	$\overline{OEA}$	$\overline{CLEAR}$	CP	An Σ of Highs	Bn† Σ of Highs	A	B	PARITY	$\overline{ERROR}$‡
A data to B bus and generate parity	L	H	X	X	Odd Even	NA	NA	A	L H	NA
B data to A bus and check parity	H	L	H	↑	NA	Odd Even	B	NA	NA	H L
Clear error flag register	X	X	L	X	X	X	X	NA	NA	H
A bus and B bus disabled §	H	H	H L H H	 ‡ ‡	X X Odd Even	X	Z	Z	Z	NC H H L
A data to B bus and generate inverted parity (Forced-error)	L	L	X	X	Odd Even	NA	NA	A	H L	NA

ERROR FLAG FUNCTION TABLE

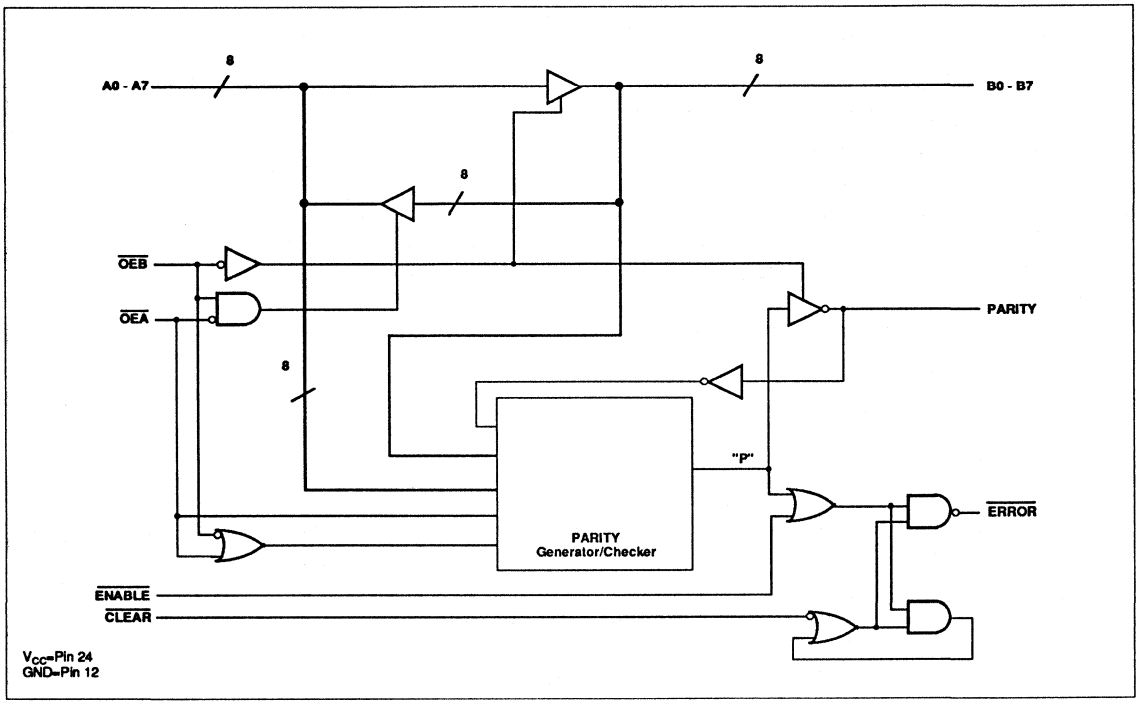
MODE	INPUTS		Internal node Point "P"	OUTPUT
	$\overline{CLEAR}$	$\overline{ENABLE}$		$\overline{ERROR}$
Transparent	L L	L L	L H	L H
Sample	H H	L L	L H	L H
Clear	L	H	X	H
Store	H H	H H	L H	L H

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care
NA = Not applicable
NC = No change
Z = High-impedance "OFF" state
† = Summation of High-level inputs includes PARITY along with Bn inputs
‡ = Output states shown assume the $\overline{ERROR}$ output was previously High
§ In this mode, the ERROR output, when clocked, shows inverted parity of the A bus
↑ = Low-to-High clock transition
‡ = Not a Low-to-High clock transition

8-bit transceiver with 9-bit parity checker/generator and flag latch (3-State)

74ABT853

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
I_{OH}	High-level output current $\overline{ERROR}$ only		V_{CC} = 4.5V; V_{OH} = 4.5V; V_I = V_{IL} or V_{IH}			20		20	µA
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

8-bit inverting transceiver with 9-bit parity checker/ generator and flag latch (3-State)

74ABT854

FEATURES

- Low static and dynamic power dissipation with high speed and high output drive
- Open-collector $\overline{\text{ERROR}}$ output
- Functionally equivalent to AMD AM29854
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT854 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT854 is an octal inverting transceiver with a parity generator/ checker and is intended for bus-oriented applications.

When Output Enable A ($\overline{\text{OEA}}$) is High, it will place the A outputs in a high impedance state. Output Enable B ($\overline{\text{OEB}}$) controls the B outputs in the same way.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to $\overline{\text{Bn}}$ or Bn to $\overline{\text{An}}$	C_L = 50pF; V_{CC} = 5V	2.9	ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	C_L = 50pF; V_{CC} = 5V	6.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

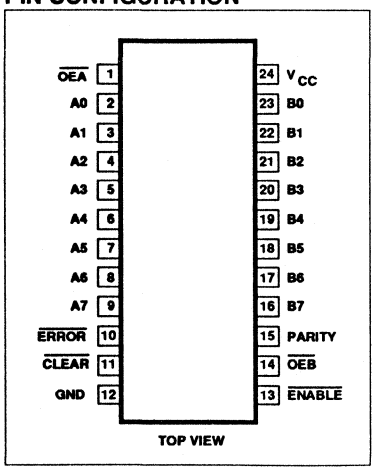
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT854N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT854D

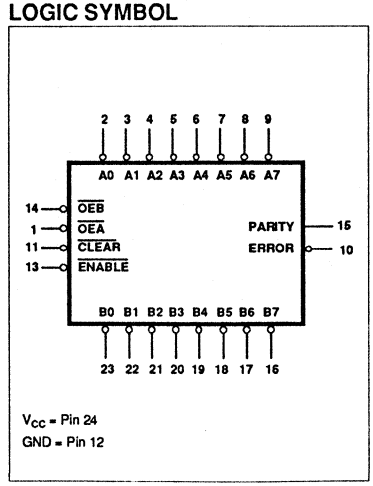
The parity generator creates an odd parity output (PARITY) when $\overline{\text{OEB}}$ is Low. When $\overline{\text{OEA}}$ is Low, the parity of the B port, including the PARITY input, is checked for odd parity. When an error is detected, the error data is sent to the input of a latch. The error data can then be passed, stored, cleared, or sampled depending on the $\overline{\text{ENABLE}}$ and $\overline{\text{CLEAR}}$ control signals.

If both $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ are Low, data will flow from the A bus to the B bus and the part is forced into an error condition which creates an inverted PARITY output. This error condition can be used by the designer for system diagnostics.

PIN CONFIGURATION



LOGIC SYMBOL



8-bit inverting transceiver with 9-bit parity checker/ generator and flag latch (3-State)

74ABT854

PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
A0 - A7	2, 3, 4, 5, 6, 7, 8, 9	A port 3-State inputs/outputs
B0 - B7	23, 22, 21, 20, 19, 18, 17, 16	B port 3-State inputs/outputs
$\overline{OEA}$	1	Enables the A outputs when Low
$\overline{OEB}$	14	Enables the B outputs when Low
PARITY	15	Parity output
$\overline{ERROR}$	10	Error output
$\overline{CLEAR}$	11	Clears the error flag register when Low
$\overline{ENABLE}$	13	Enable input (active low)
GND	12	Ground (0V)
V_{CC}	24	Positive supply voltage

FUNCTION TABLE

MODE	INPUTS						OUTPUT AND I/O			
	$\overline{OEB}$	$\overline{OEA}$	$\overline{CLEAR}$	CP	An Σ of Highs	Bn† Σ of Highs	A	B	PARITY	$\overline{ERROR}$‡
A data to B bus and generate parity	L	H	X	X	Odd Even	NA	NA	$\overline{A}$	L H	NA
B data to A bus and check parity	H	L	H	↑	NA	Odd Even	$\overline{B}$	NA	NA	H L
Clear error flag register	X	X	L	X	X	X	X	NA	NA	H
A bus and B bus disabled §	H	H	H L H H	 ‡ ‡	X X Odd Even	X	Z	Z	Z	NC H H L
A data to B bus and generate inverted parity (Forced-error)	L	L	X	X	Odd Even	NA	NA	$\overline{A}$	H L	NA

ERROR FLAG FUNCTION TABLE

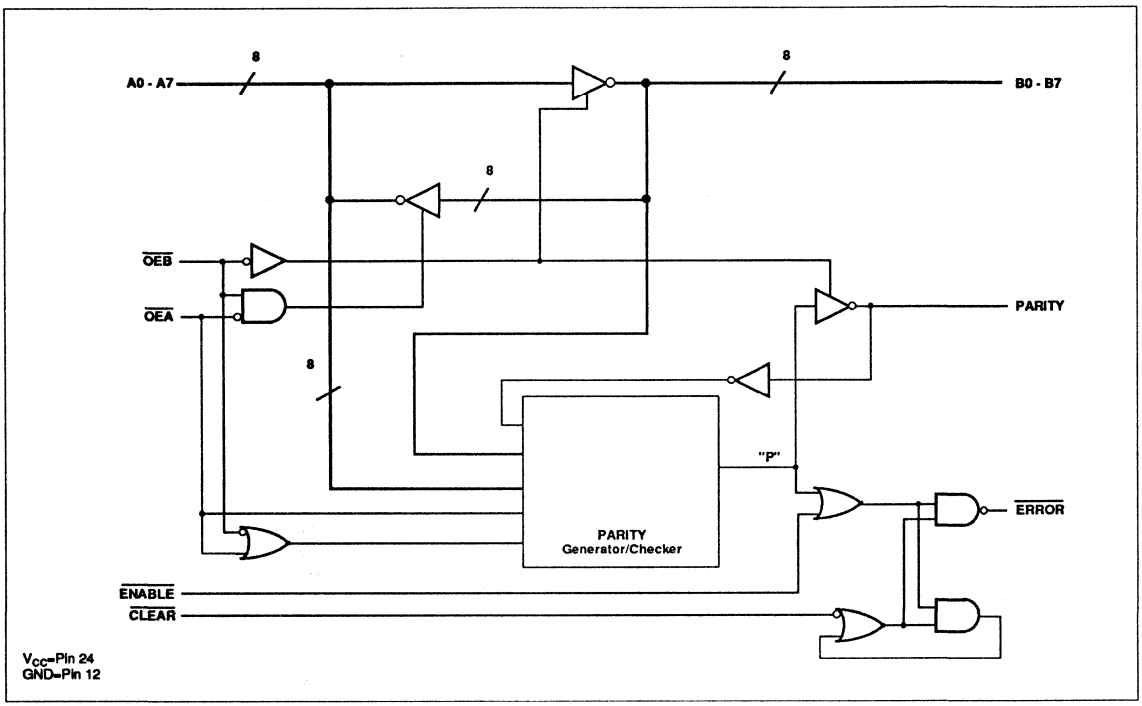
MODE	INPUTS		Internal node Point "P"	OUTPUT
	$\overline{CLEAR}$	$\overline{ENABLE}$		$\overline{ERROR}$
Transparent	L L	L L	L H	L H
Sample	H H	L L	L H	L H
Clear	L	H	X	H
Store	H H	H H	L H	L H

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care
NA = Not applicable
NC = No change
Z = High-impedance "OFF" state
† = Summation of High-level inputs includes PARITY along with Bn inputs
‡ = Output states shown assume the $\overline{ERROR}$ output was previously High
§ In this mode, the ERROR output, when clocked, shows inverted parity of the A bus
↑ = Low-to-High clock transition
‡ = Not a Low-to-High clock transition

8-bit inverting transceiver with 9-bit parity checker/ generator and flag latch (3-State)

74ABT854

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
I_{OH}	High-level output current $\overline{ERROR}$ only		V_{CC} = 4.5V; V_{OH} = 4.5V; V_I = V_{IL} or V_{IH}			20		20	µA
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

10-bit bus transceiver (3-State) 74ABT861

FEATURES

- Provide high performance bus interface buffering for wide data/address paths or buses carrying parity
- Buffered control inputs for light loading, or increased fan-in as required with MOS microprocessors
- Slim Dip 300 mil package
- Broadside pinout compatible with AMD AM 29861
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT861 bus transceiver provides high performance bus interface buffering for wide data/address paths of buses carrying parity.

The 'ABT861 10-bit bus transceiver has NOR-ed transmit and receive output enables for maximum control flexibility.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn, or Bn to An	C_L = 50pF; V_{CC} = 5V	4.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

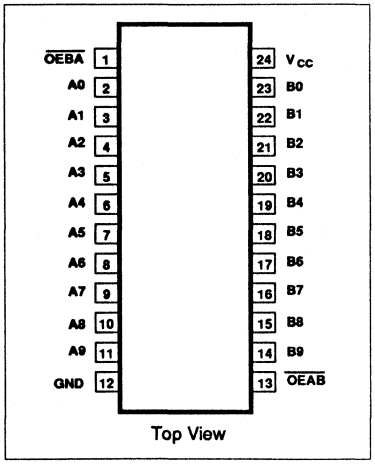
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP	-40°C to +85°C	74ABT861N
24-pin plastic SOL	-40°C to +85°C	74ABT861D

PIN DESCRIPTION

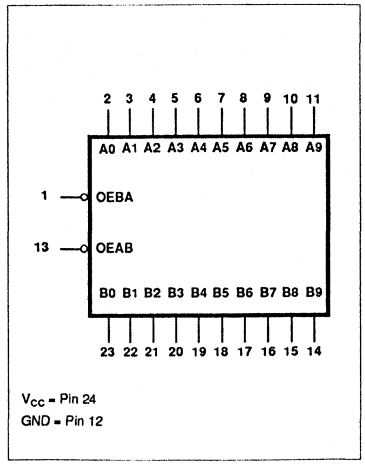
PIN NUMBER	SYMBOL	NAME AND FUNCTION
13	$\overline{OEAB}$	A side to B side ouput enable input (active Low)
2, 3, 4, 5, 6 7, 8, 9, 10, 11	A0 - A8	Data inputs/outputs (A side)
14, 15, 16, 17, 18 19, 20, 21, 22, 23	B0 - B8	Data inputs/outputs (B side)
1	$\overline{OEBA}$	B side to A side ouput enable input (active Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

PIN CONFIGURATION

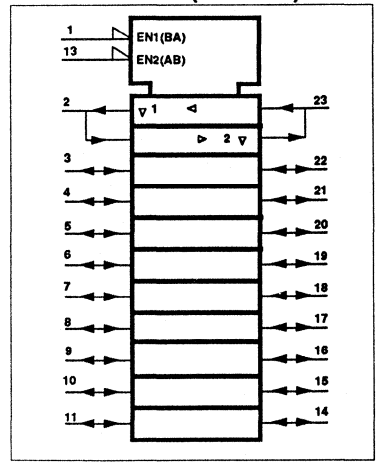


Top View

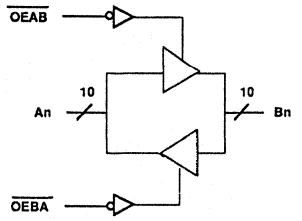
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		MODE
$\overline{OEB}$	$\overline{OEA}$	
L	H	A data to B bus
H	L	B data to A bus
H	H	Z

H = High voltage level steady state
L = Low voltage level steady state
Z = High-impedance "OFF" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		30	38		38	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

9-bit bus transceiver (3-State) 74ABT863

FEATURES

- Provide high performance bus interface buffering for wide data/address paths or buses carrying parity
- Buffered control inputs for light loading, or increased fan-in as required with MOS microprocessors
- Slim Dip 300 mil package
- Broadside pinout compatible with AMD AM 29863
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT863 Bus Transceiver provides high performance bus interface buffering for wide data/address paths of buses carrying parity. The 'ABT863 9-bit Bus Transceiver has NOR-ed transmit and receive output enables for maximum control flexibility.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn, or Bn to An	C_L = 50pF; V_{CC} = 5V	4.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

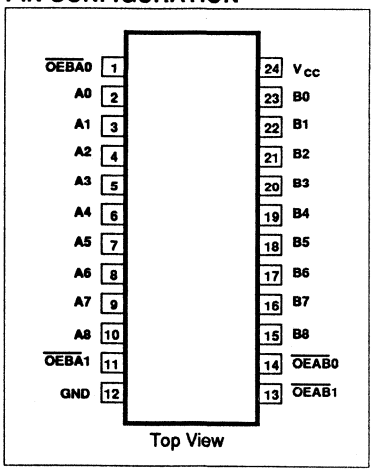
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP	-40°C to +85°C	74ABT863N
24-pin plastic SOL	-40°C to +85°C	74ABT863D

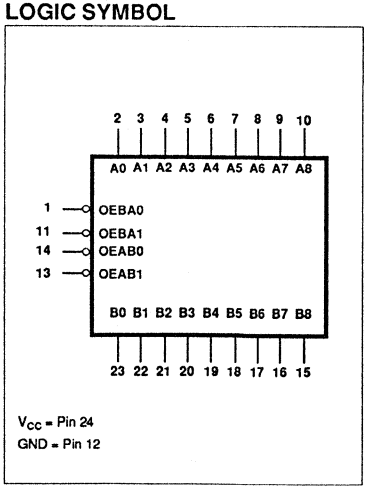
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
14, 13	$\overline{OEAB0}$, $\overline{OEAB1}$	Direction control input
2, 3, 4, 5 6, 7, 8, 9, 10	A0 - A7	Data inputs/outputs (A side)
15, 16, 17, 18 19, 20, 21, 22, 23	B0 - B7	Data inputs/outputs (B side)
1, 11	$\overline{OEBA0}$, $\overline{OEBA1}$	Ouput enable
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

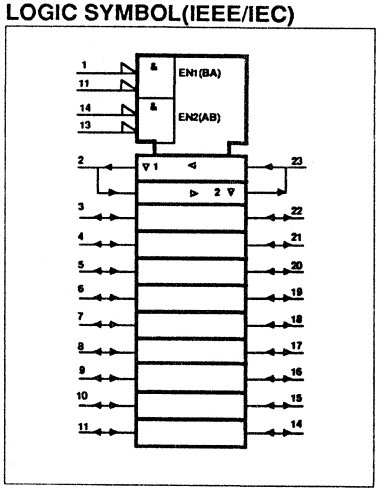
PIN CONFIGURATION



LOGIC SYMBOL

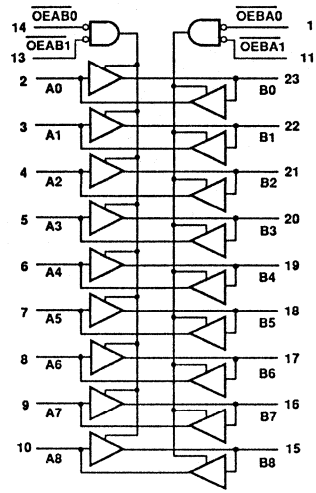


LOGIC SYMBOL(IEEE/IEC)



9-bit bus transceiver (3-State) 74ABT863

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OPERATING MODES
$\overline{OEAB0}$	$\overline{OEAB1}$	$\overline{OEBA0}$	$\overline{OEBA1}$	
L L	L L	H X	X H	A data to B bus A data to B bus
H X	X H	L L	L L	B bus to A data B bus to A data
H	H	H	H	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
I_{IH} + I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		28	34		34	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

9-bit dual latch transceiver with 8-bit parity generator/checker (3-State)

74ABT899

FEATURES

- Symmetrical (A and B bus functions are identical)
- Selectable generate parity or "feed-through" parity for A-to-B and B-to-A directions
- Independent transparent latches for A-to-B and B-to-A directions
- Selectable ODD/$\overline{\text{EVEN}}$ parity
- Continuously checks parity of both A bus and B bus latches as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$
- Ability to simultaneously generate and check parity
- Can simultaneously read/latch A and B bus data
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT899 is a 9-bit to 9-bit parity transceiver with separate transparent latches for the A bus and B bus. Either bus can generate or check parity. The parity bit can be fed-through with no change or the generated parity can be substituted with the $\overline{\text{SEL}}$ input. Parity error checking of the A and B bus latches is continuously provided with $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$, even with both buses in 3-State.

The device has a guaranteed current sinking capability of 32mA for the A-bus and 64 mA for the B-bus. Otherwise, the part is symmetrical (A and B bus functions are identical).

The 74ABT899 features independent latch enables for the A and B bus latches, a select pin for ODD/$\overline{\text{EVEN}}$ parity, and separate error signal output pins for checking parity.

FUNCTIONAL DESCRIPTION:

The 74ABT899 has three principal modes of operation which are outlined below. All modes apply to both the A-to-B and B-to-A directions.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	2.9	ns
t_{PLH} t_{PHL}	Propagation delay An to $\overline{\text{ERRA}}$	C_L = 50pF; V_{CC} = 5V	6.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil)	-40°C to +85°C	74ABT899N
28-pin plastic SOL (300mil)	-40°C to +85°C	74ABT899D

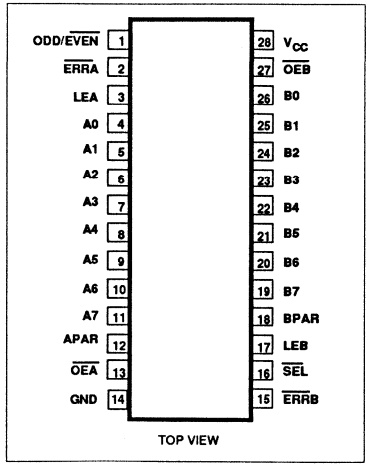
Transparent latch, Generate parity, Check A and B bus parity:
Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEA and LEB are High and the Mode Select ($\overline{\text{SEL}}$) is Low, the parity generated from A0-A7 and B0-B7 can be checked and monitored by $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$. (Fault detection on both input and output buses.)

Transparent latch, Feed-through parity, Check A and B bus parity:
Bus A (B) communicates to Bus B (A) in a feed-through mode if $\overline{\text{SEL}}$ is High. Parity is still generated and checked as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ and can be used as an interrupt to signal a data/parity bit error to the CPU.

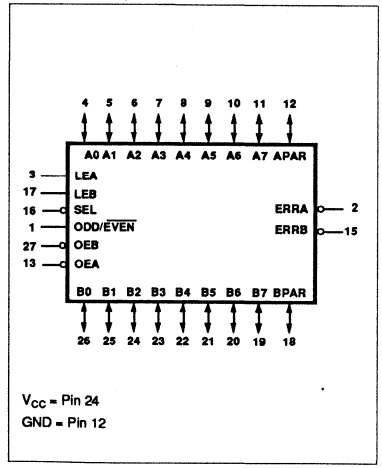
Latched input, Generate/Feed-through parity, Check A (and B) bus parity:
Independent latch enables (LEA and LEB) allow other permutations of:

- Transparent latch / 1 bus latched / both buses latched
- Feed-through parity / generate parity
- Check in bus parity / check out bus parity / check in and out bus parity

PIN CONFIGURATION



LOGIC SYMBOL



9-bit dual latch transceiver with 8-bit parity generator/checker (3-State)

74ABT899

PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
A0 - A7	4, 5, 6, 7, 8, 9, 10, 11	Latched A port inputs/outputs (3-State)
B0 - B7	19, 20, 21, 22, 23, 24, 25, 26	Latched B port inputs/outputs (3-State)
APAR	12	A bus parity input (3-State)
BPAR	18	B bus parity input (3-State)
ODD/$\overline{\text{EVEN}}$	1	Parity select input (Low for even parity)
$\overline{\text{GBA}}$, $\overline{\text{GAB}}$	13, 27	Ouput Enable inputs (Gate A to B, B to A)
$\overline{\text{SEL}}$	16	Mode select input (Low for generate)
LEA, LEB	3, 17	Latch Enable inputs (Low for latch)
$\overline{\text{ERRA}}$, $\overline{\text{ERRB}}$	2, 15	Error signal outputs (active Low)
GND	14	Ground (0V)
V_{CC}	28	Positive supply voltage

FUNCTION TABLE

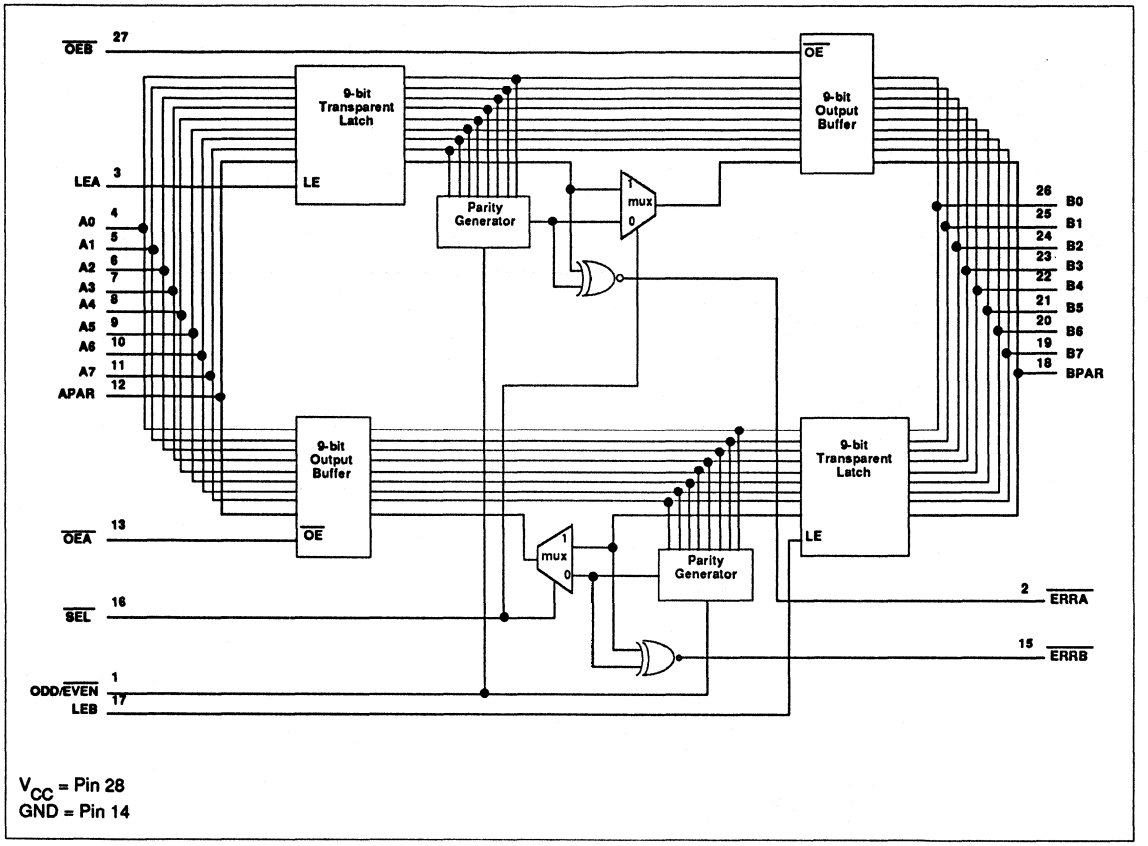
INPUTS					OPERATING MODE
$\overline{\text{OEB}}$	$\overline{\text{OEA}}$	$\overline{\text{SEL}}$	LEA	LEB	
H	H	X	X	X	3-State A bus and B bus (Input A & B simultaneously)
H	L	L	L	H	B → A, Transparent B latch, Generate parity from B0-B7, Check B bus parity
H	L	L	H	H	B → A, Transparent A & B latch, Generate parity from B0-B7, Check A & B bus parity
H	L	L	X	L	B → A, B bus latched, Generate parity from latched B0-B7 data, Check B bus parity
H	L	H	X	H	B → A, Transparent B latch, Parity feed-through, Check B bus parity
H	L	H	H	H	B → A, Transparent A & B latch, Parity feed-through, Check A & B bus parity
L	H	L	H	X	A → B, Transparent A latch, Generate parity from A0-A7, Check A bus parity
L	H	L	H	H	A → B, Transparent A & B latch, Generate parity from A0-A7, Check A & B bus parity
L	H	L	L	X	A → B, A bus latched, Generate parity from latched A0-A7 data, Check A bus parity
L	H	H	H	L	A → B, Transparent A latch, Parity feed-through, Check A bus parity
L	H	H	H	H	A → B, Transparent A & B latch, Parity feed-through, Check A & B bus parity
L	L	X	X	X	Output to A bus and B bus (NOT ALLOWED)

H = High voltage level
L = Low voltage level
X = Don't care

9-bit dual latch transceiver with 8-bit parity generator/checker (3-State)

74ABT899

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9-bit dual latch transceiver with 8-bit parity generator/checker (3-State) — 74ABT899

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		28	34		34	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Octal registered transceiver (3-State)

74ABT2952

FEATURES

- 8-bit registered transceiver
- Independent registers for A and B buses
- AM2952 functional equivalent
- Outputs sink 64mA and source 32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT2952 is an 8-bit Registered Transceiver. Two 8-bit back to back registers store data flowing in both directions between two bi-directional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	C_L = 50pF; V_{CC} = 5V	5.7	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

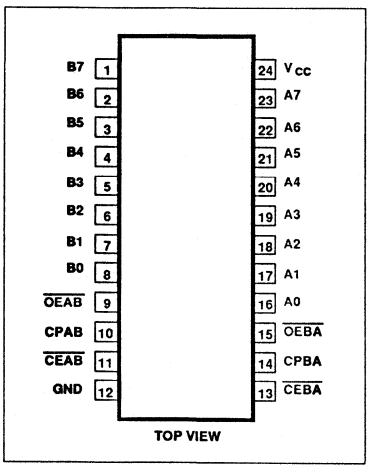
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT2952N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT2952D

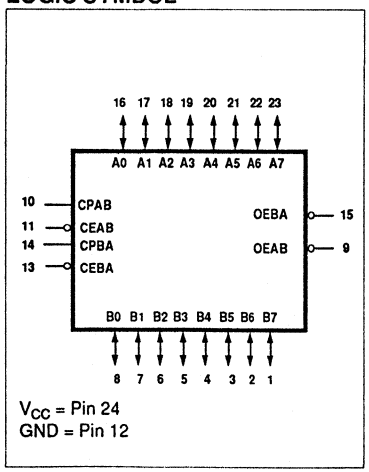
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
10, 14	CPAB / CPBA	Clock input A to B / Clock input B to A
11, 13	$\overline{CEAB}$ / $\overline{CEBA}$	Clock enable input A to B / Clock enable B to A
16, 17, 18, 19 20, 21, 22, 23	A0 - A7	Data inputs/outputs (A side)
1, 2, 3, 4 5, 6, 7, 8	B0 - B7	Data inputs/outputs (B side)
9, 15	$\overline{OEAB}$ / $\overline{OEBA}$	Output enable input
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

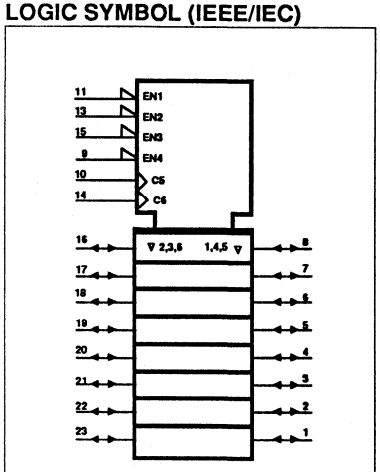
PIN CONFIGURATION DIP



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal registered transceiver (3-State) 74ABT2952

FUNCTION TABLE for Register An or Bn

INPUTS			INTERNAL Q	OPERATING MODE
An or Bn	CPXX	$\overline{CEXX}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	

H = High voltage level
L = Low voltage level
↑ = Low-to-High transition
X = Don't care
XX = AB or BA
NC = No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL Q	An or Bn OUTPUTS	OPERATING MODE
$\overline{OEXX}$			
H	X	Z	Disable outputs
L	L	L	Enable outputs
L	H	H	

H = High voltage level
L = Low voltage level
X = Don't care
XX = AB or BA
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

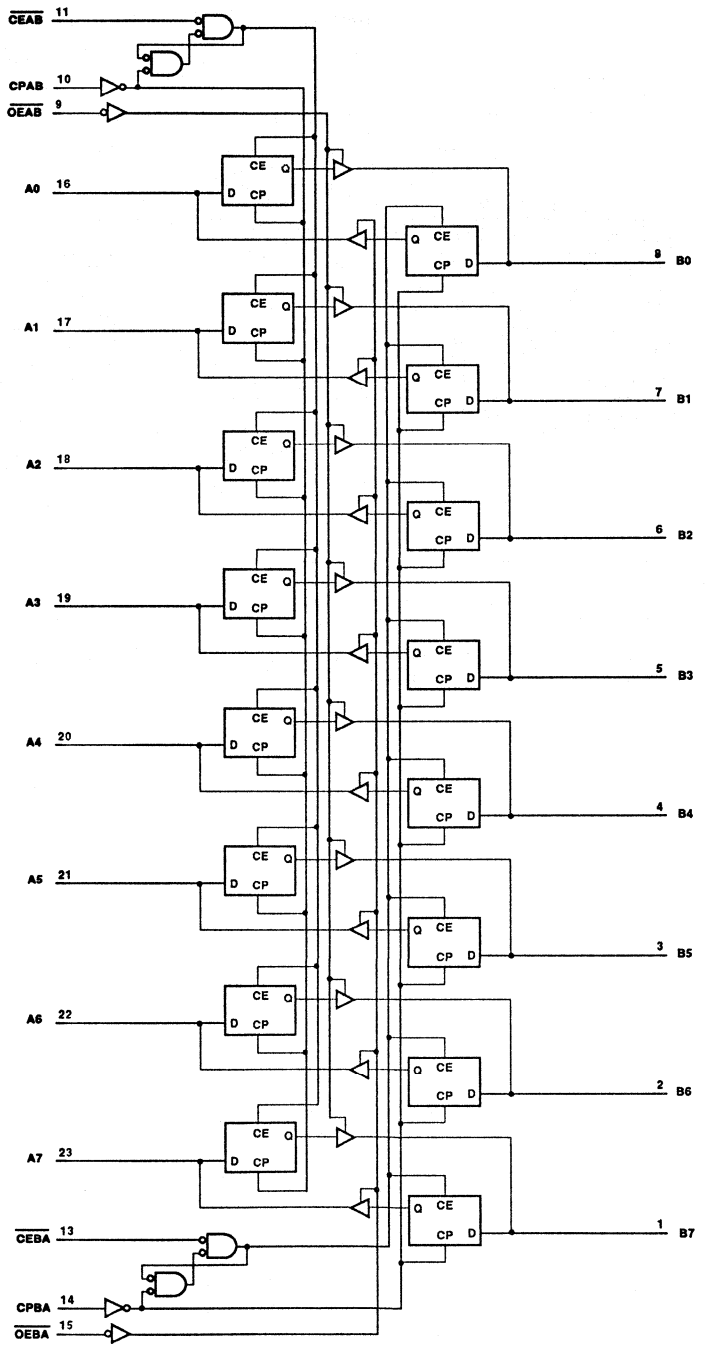
SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
I_{IH} + I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC ELECTRICAL CHARACTERISTICS

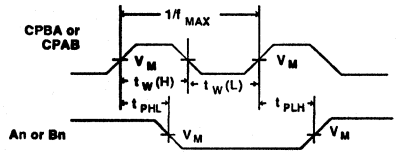
GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V			T_{amb} = -40°C to +85°C, V_{CC} = 5V±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	150			150		ns
t_{PLH} t_{PHL}	Propagation delay CPBA to An, CPAB to Bn	Waveform 1	2.0 2.5	5.1 5.7	6.6 7.2	2.0 2.5	7.6 8.2	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	Waveform 3 Waveform 4	1.0 2.2	3.3 4.7	4.8 6.2	1.0 2.2	5.8 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	Waveform 3 Waveform 4	2.0 1.5	6.1 5.6	7.6 7.1	2.0 1.5	8.1 7.6	ns

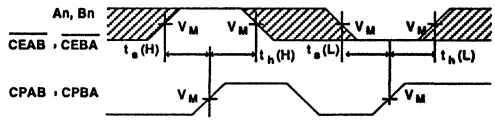
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V			T_{amb} = -40°C to +85°C, V_{CC} = 5V±0.5V		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time An to CPAB or Bn to CPBA	Waveform 2	4.5 3.5	3.1 1.9		4.5 3.5		ns
$t_h(H)$ $t_h(L)$	Hold time An to CPAB or Bn to CPBA	Waveform 2	0.0 0.0	-1.5 -2.8		0.0 0.0		ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{CEAB}$ to CPAB, $\overline{CEBA}$ to CPBA	Waveform 2	4.0 3.0	2.6 1.8		4.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time $\overline{CEAB}$ to CPAB, $\overline{CEBA}$ to CPBA	Waveform 2	0.0 0.0	-1.5 -1.5		0.0 0.0		ns
$t_w(H)$ $t_w(L)$	CPAB or CPBA pulse width, High or Low	Waveform 1	3.0 3.5	1.9 2.6		3.0 3.5		ns

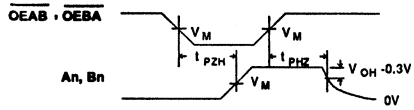
AC WAVEFORMS



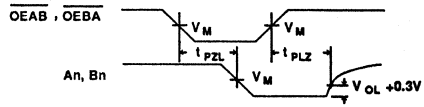
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup And Hold Times



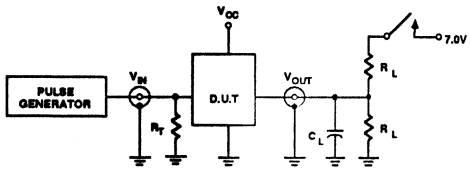
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded area indicate when the input is permitted to change for predictable output

TEST CIRCUIT AND WAVEFORMS



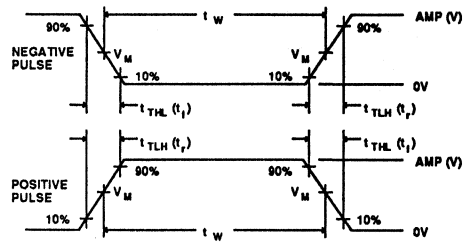
Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

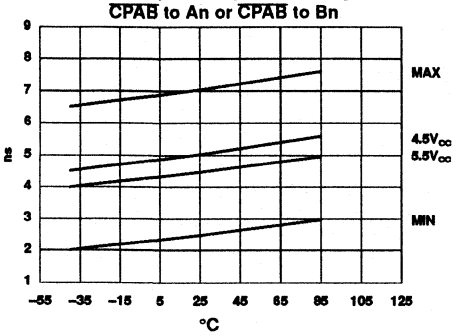
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



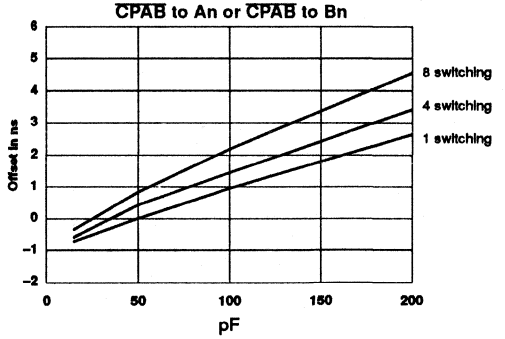
V_M = 1.5V
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

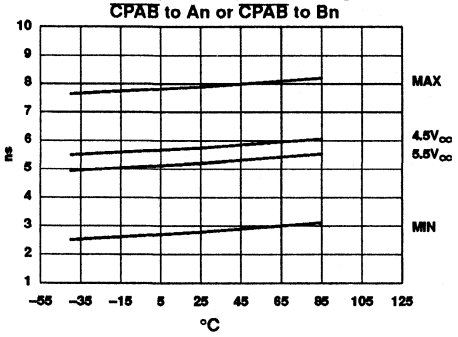
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{CPAB}$ to An or $\overline{CPAB}$ to Bn



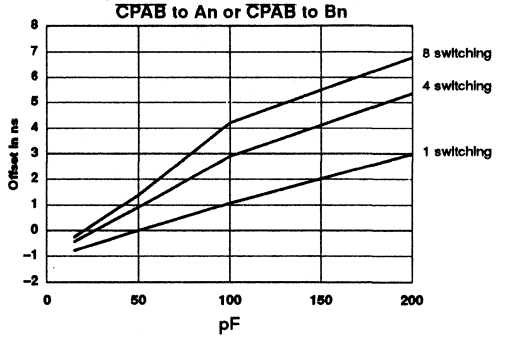
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
$\overline{CPAB}$ to An or $\overline{CPAB}$ to Bn



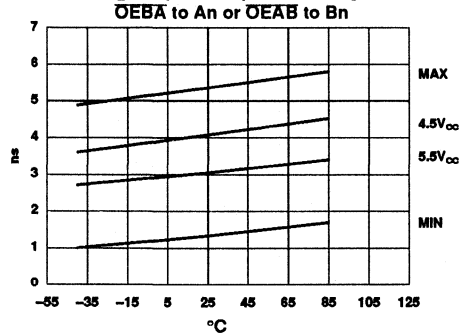
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{CPAB}$ to An or $\overline{CPAB}$ to Bn



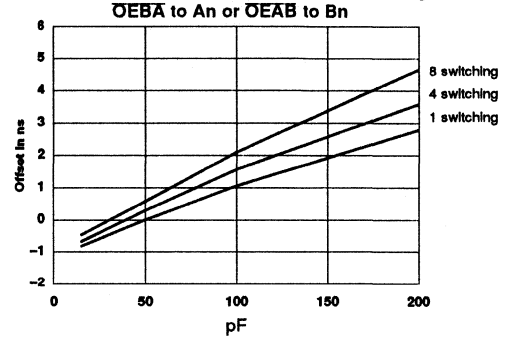
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
$\overline{CPAB}$ to An or $\overline{CPAB}$ to Bn



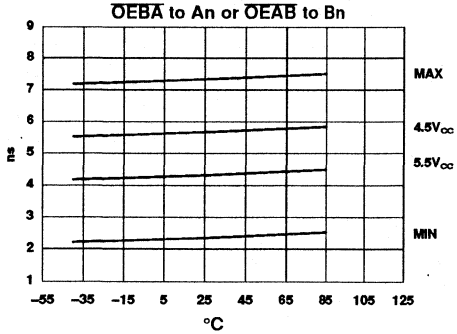
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



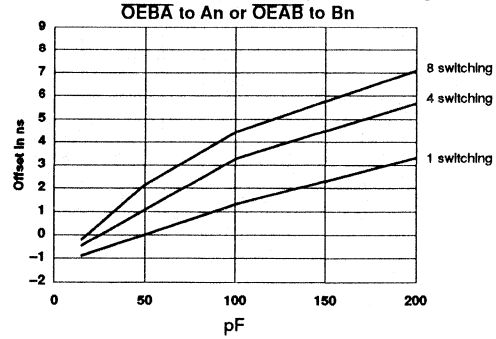
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



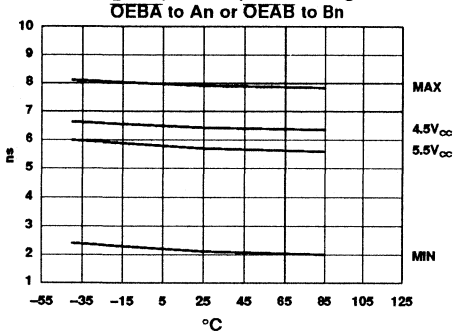
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



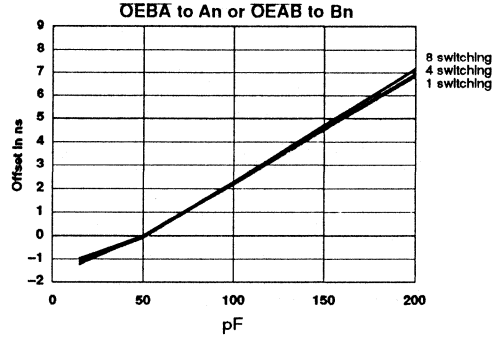
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



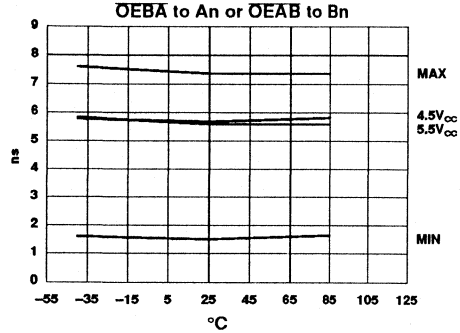
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



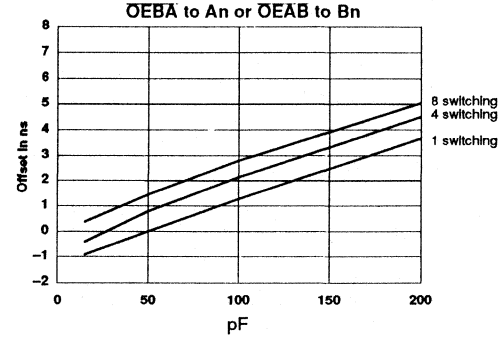
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn

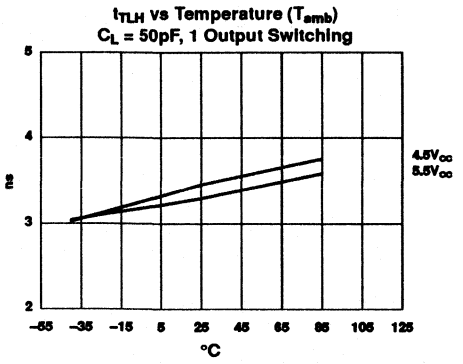


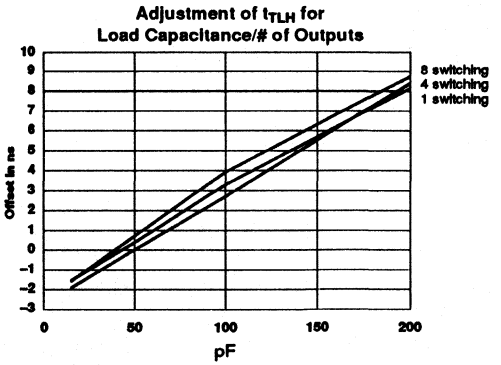
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn

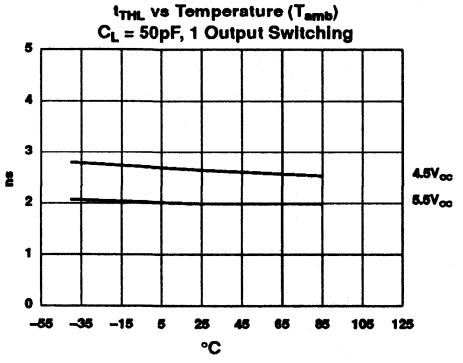


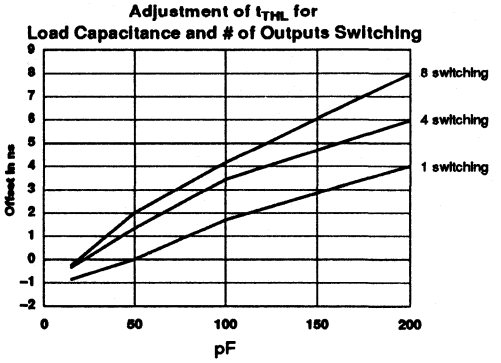
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn

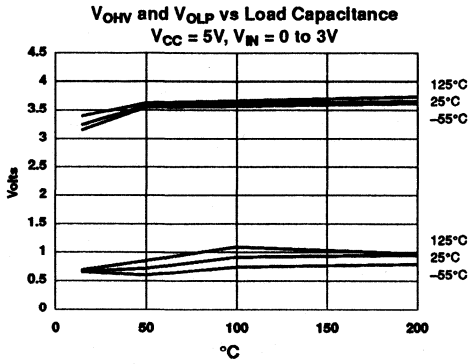


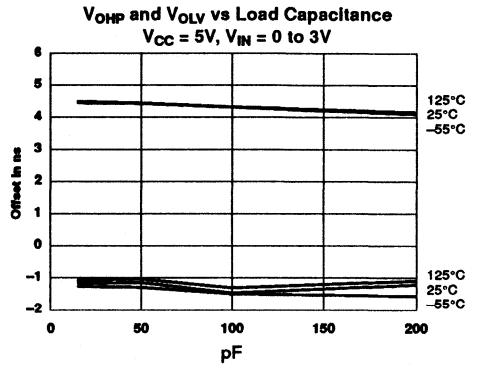

t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V$_{CC}$
5.5V$_{CC}$


Adjustment of t_{TLH} for
Load Capacitance/# of Outputs
Offset in ns
pF
8 switching
4 switching
1 switching


t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V$_{CC}$
5.5V$_{CC}$


Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
8 switching
4 switching
1 switching


V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
Volts
°C
125°C
25°C
–55°C
125°C
25°C
–55°C


V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
Offset in ns
pF
125°C
25°C
–55°C
125°C
25°C
–55°C

Octal registered transceiver, inverting (3-State) — 74ABT2953

FEATURES

- 8-bit registered inverting transceivers
- Separate clock, clock enable and 3-State enable provided for each register
- AM2953 functional equivalent
- Outputs sink 64mA and source 32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT2953 is an 8-bit registered inverting transceiver. Two 8-bit back to back registers store data flowing in both directions between two bi-directional busses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-state output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to $\overline{A}$nor $\overline{B}$n	C_L = 50pF; V_{CC} = 5V	5.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

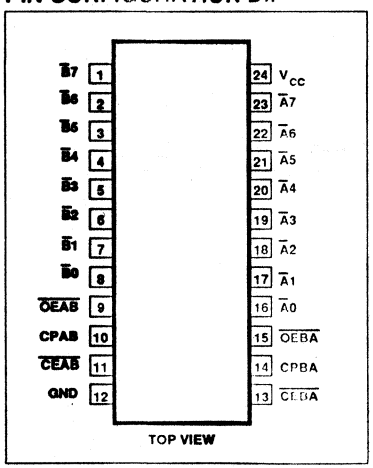
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT2953N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT2953D

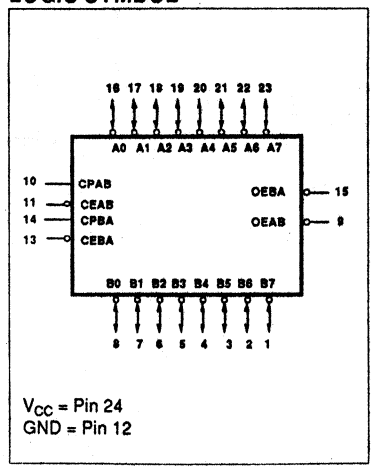
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
10, 14	CPAB / CPBA	Clock input A to B / Clock input B to A
11, 13	$\overline{CEAB}$ / $\overline{CEBA}$	Clock enable input A to B / Clock enable B to A
16, 17, 18, 19 20, 21, 22, 23	$\overline{A}$0 - $\overline{A}$7	Data inputs/outputs (A side)
1, 2, 3, 4 5, 6, 7, 8	$\overline{B}$0 - $\overline{B}$7	Data inputs/outputs (B side)
9, 15	$\overline{OEAB}$ / $\overline{OEBA}$	Ouput enable input
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

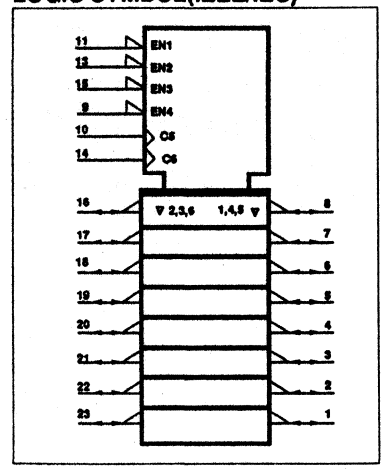
PIN CONFIGURATION DIP



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Octal registered transceiver, inverting (3-State) 74ABT2953

FUNCTION TABLE for Register An or Bn

INPUTS			INTERNAL Q	OPERATING MODE
An or Bn	CPXX	$\overline{CEXX}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	

H= High voltage level
L= Low voltage level
↑ =Low-to-High transition
X=Don't care
XX=AB or BA
NC=No change

FUNCTION TABLE for Output Enable

INPUTS $\overline{OEXX}$	INTERNAL Q	An or Bn OUTPUTS	OPERATING MODE
H	X	Z	Disable outputs
L	L	H	Enable outputs
L	H	L	

H= High voltage level
L= Low voltage level
X=Don't care
XX=AB or BA
Z =High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

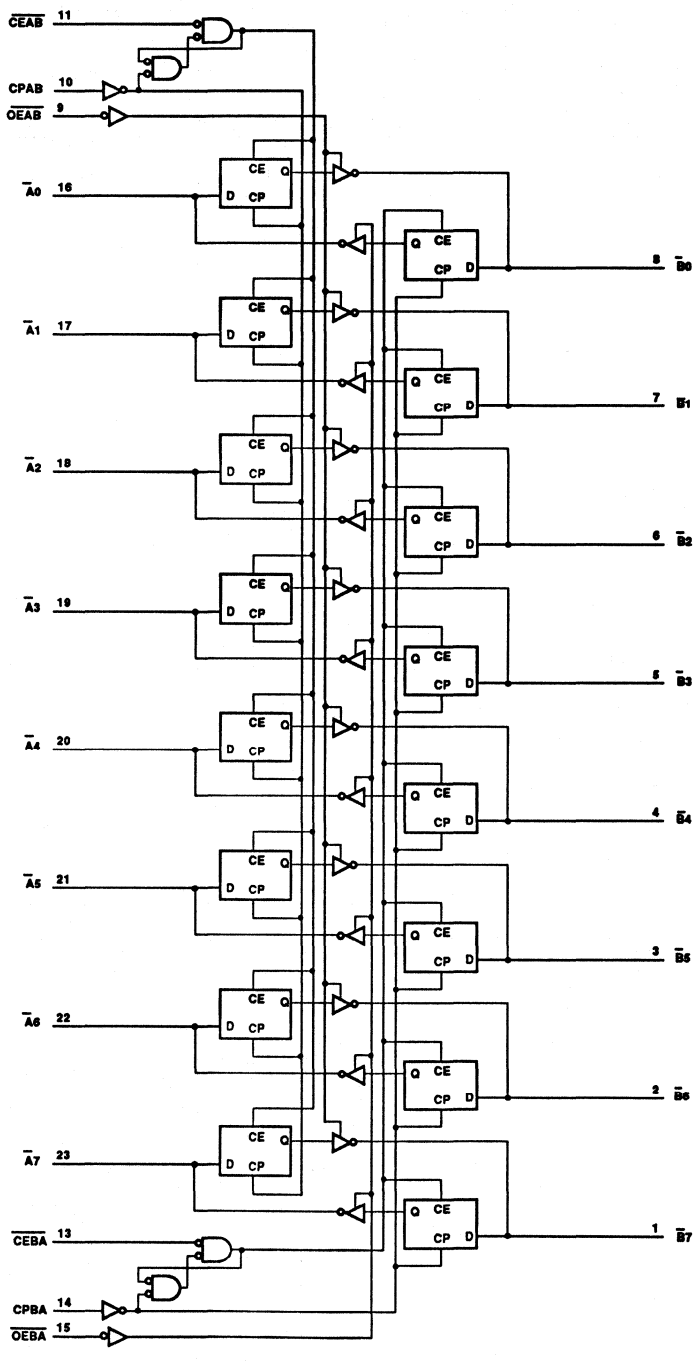
SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
I_{IH} + I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC ELECTRICAL CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

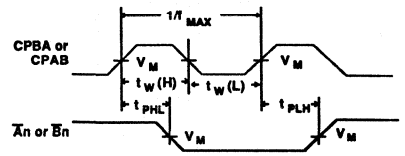
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5.0V			T_{amb} = -40°C to +85°C, V_{CC} = 5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	150	200		150		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA or CPAB to $\overline{An}$ or $\overline{Bn}$	Waveform 1	2.0 2.5	5.1 5.7	6.6 7.2	2.0 2.5	7.6 8.2	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ or $\overline{OEAB}$ to $\overline{An}$ or $\overline{Bn}$	Waveform 3 Waveform 4	1.0 2.2	3.3 4.7	4.8 6.2	1.0 2.2	5.8 7.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ or $\overline{OEAB}$ to $\overline{An}$ or $\overline{Bn}$	Waveform 3 Waveform 4	2.0 1.5	6.1 5.6	7.6 7.1	2.0 1.5	8.1 7.6	ns

AC SETUP REQUIREMENTS

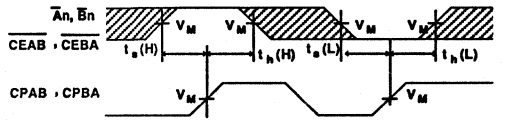
GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5.0V			T_{amb} = -40°C to +85°C, V_{CC} = 5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{An}$ or $\overline{Bn}$ to CPAB or CPBA	Waveform 2	4.0 3.0	2.5 1.5		4.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{An}$ or $\overline{Bn}$ to CPAB or CPBA	Waveform 2	0.0 0.0	-1.0 -2.0		0.0 0.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEAB}$,$\overline{CEBA}$ to CPAB , CPBA	Waveform 2	3.5 2.5	2.0 1.2		3.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEAB}$,$\overline{CEBA}$ to CPAB , CPBA	Waveform 2	0.0 0.0	-1.0 -1.0		0.0 0.0		ns
$t_w(H)$ $t_w(L)$	CPAB or CPBA Pulse width, High or Low	Waveform 1	3.0 3.5	2.0 2.6		3.0 3.5		ns

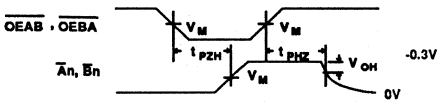
AC WAVEFORMS



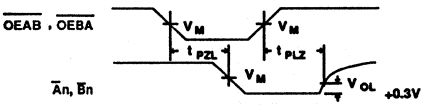
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup And Hold Times



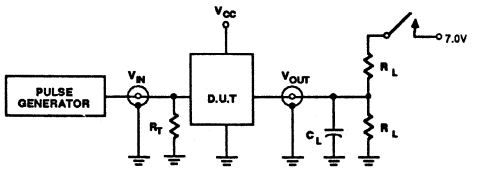
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded area indicate when the input is permitted to change for predictable output

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

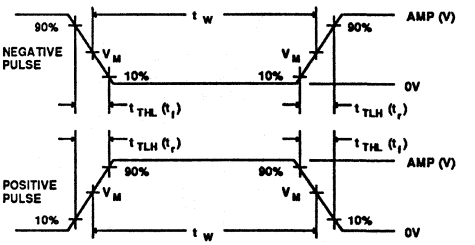
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

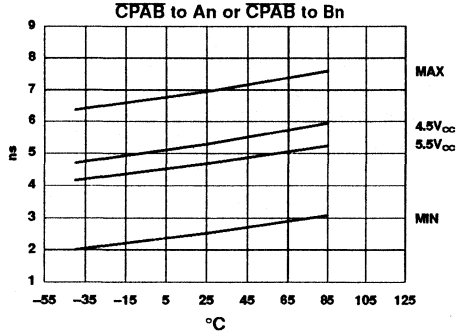


V_M = 1.5V

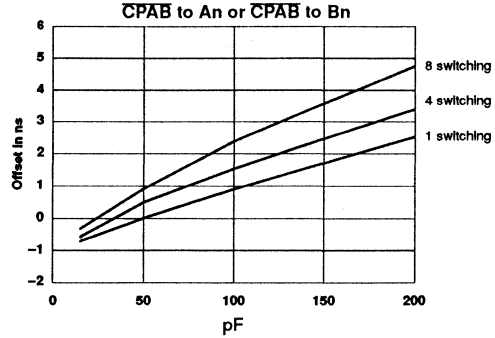
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

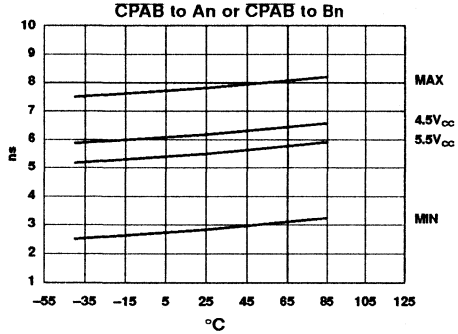
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{CPAB}$ to An or $\overline{CPAB}$ to Bn



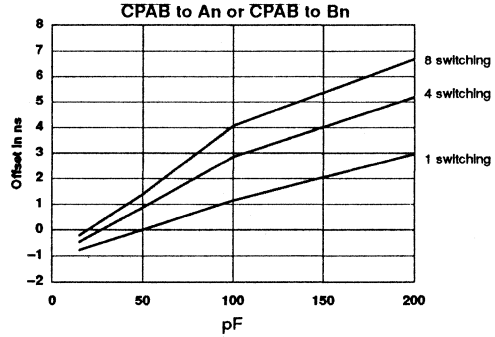
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
$\overline{CPAB}$ to An or $\overline{CPAB}$ to Bn



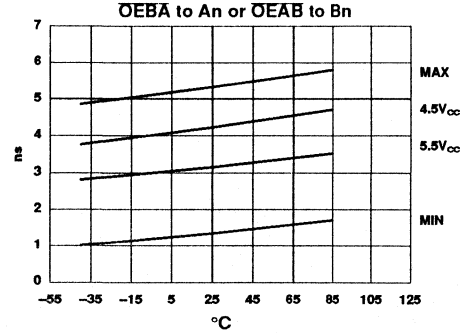
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{CPAB}$ to An or $\overline{CPAB}$ to Bn



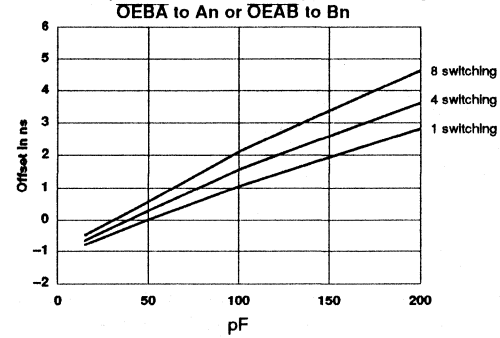
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
$\overline{CPAB}$ to An or $\overline{CPAB}$ to Bn



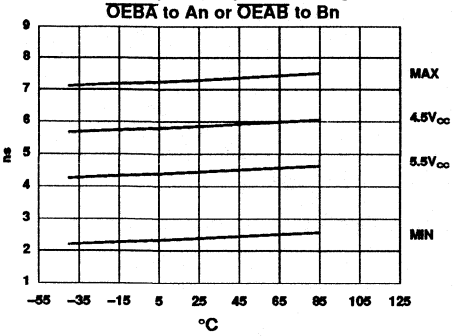
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



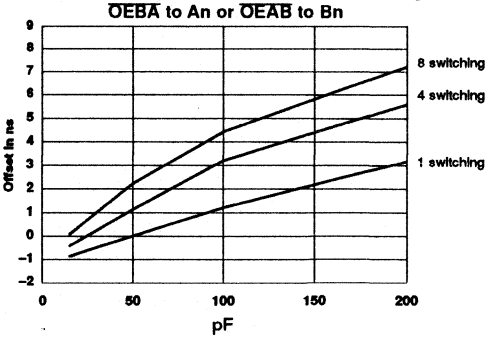
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



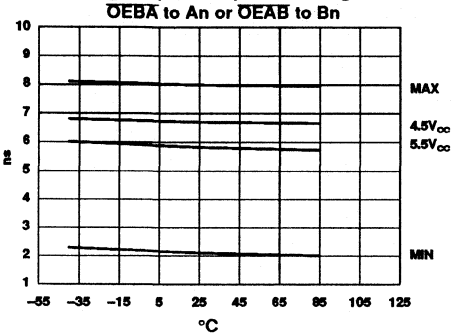
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



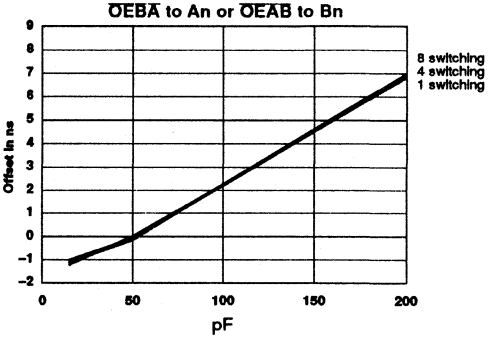
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



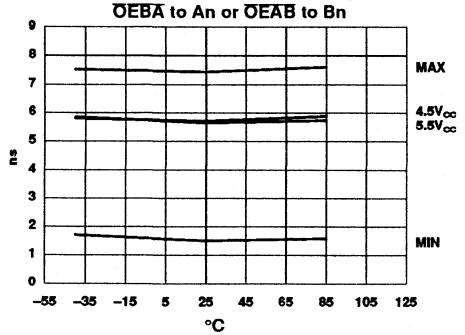
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



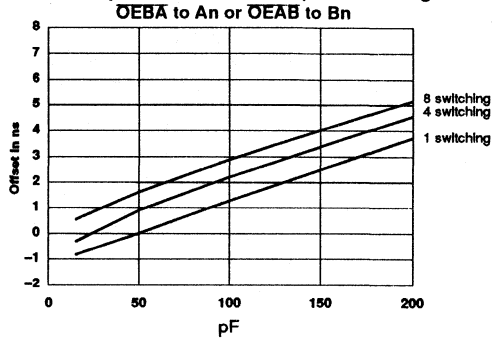
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



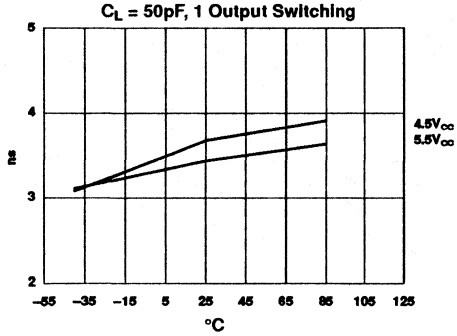
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



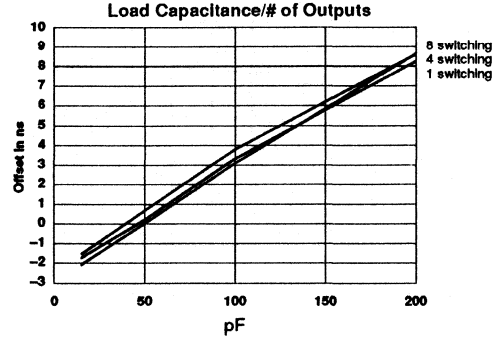
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn



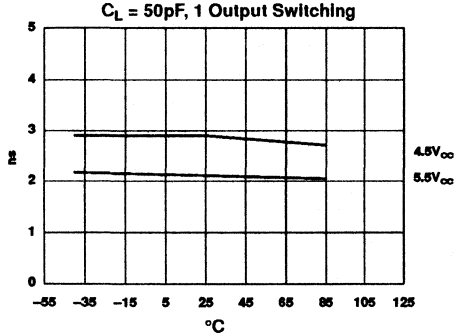
t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



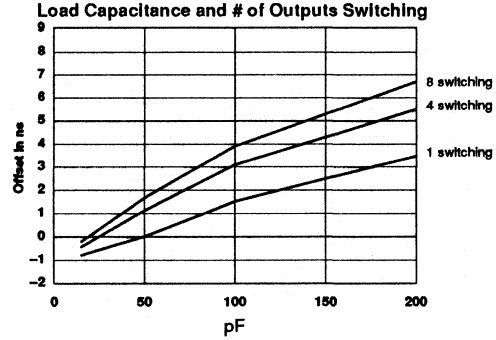
Adjustment of t_{TLH} for
Load Capacitance/# of Outputs



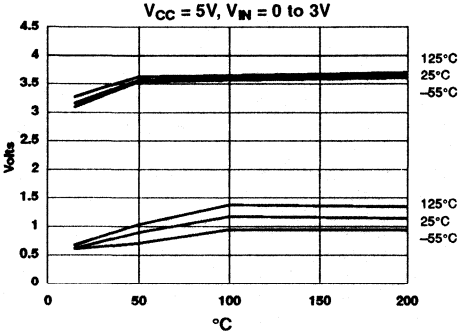
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



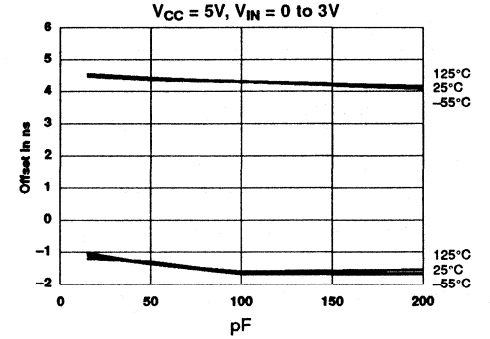
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching



V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



Section 5
MULTIBYTE Bus Interface Logic Data Sheets

INDEX

Dual octal registered transceiver (3-State)

MB2052

FEATURES

- 16-bit registered transceiver
- Multiple V_{CC} and GND pins minimize switching noise
- Independent registers for A and B buses
- AM2952 functional equivalent
- Outputs sink 64mA and source 32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	C_L = 50pF; V_{CC} = 5V	5.7	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

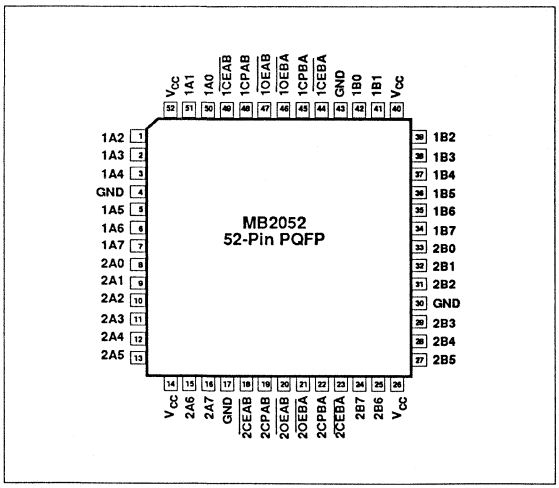
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
52-pin plastic QFP	-40°C to +85°C	MB2052B

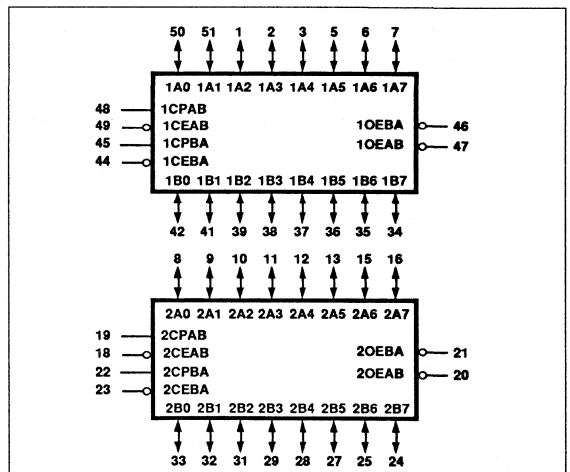
DESCRIPTION

The MB2052 is a dual octal registered transceiver. Two 8-bit registers store data flowing in both directions between two bi-directional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

PIN CONFIGURATION



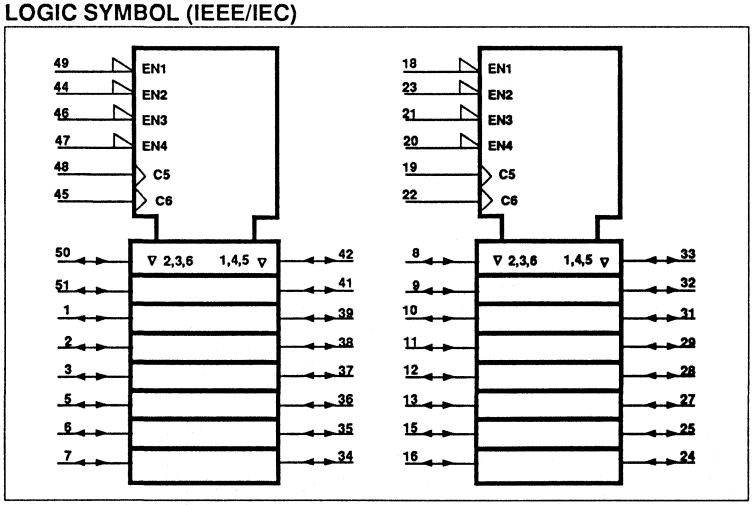
LOGIC SYMBOL



PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1A0 - 1A7, 2A0 - 2A7	50, 51, 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16	Data inputs
1B0 - 1B7, 2B0 - 2B7	42, 41, 39, 38, 37, 36, 35, 34, 33, 32, 31, 29, 28, 27, 25, 24	Data outputs
$1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$	47, 46, 20, 21	Output enables
$1\overline{CEAB}$, $1\overline{CEBA}$, $2\overline{CEAB}$, $2\overline{CEBA}$	49, 44, 18, 23	Clock enable inputs A to B / Clock enable inputs B to A
1CPAB, 1CPBA, 2CPAB, 2CPBA	48, 45, 19, 22	Clock inputs A to B / Clock inputs B to A
GND	4, 17, 30, 43	Ground (0V)
V_{CC}	14, 26, 40, 52	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



Dual octal registered transceiver (3-State) MB2052

FUNCTION TABLE for Register nAx or nBx

INPUTS			INTERNAL Q	OPERATING MODE
nAx or nBx	nCPXX	$\overline{1CEXX}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	

H = High voltage level
L = Low voltage level
↑ = Low-to-High transition
X = Don't care
XX = AB or BA
NC = No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL Q	An or Bn OUTPUTS	OPERATING MODE
$\overline{nOEXX}$			
H	X	Z	Disable outputs
L	L	L	Enable outputs
L	H	H	

H = High voltage level
L = Low voltage level
X = Don't care
XX = AB or BA

ABSOLUTE MAXIMUM RATINGS[1, 2]

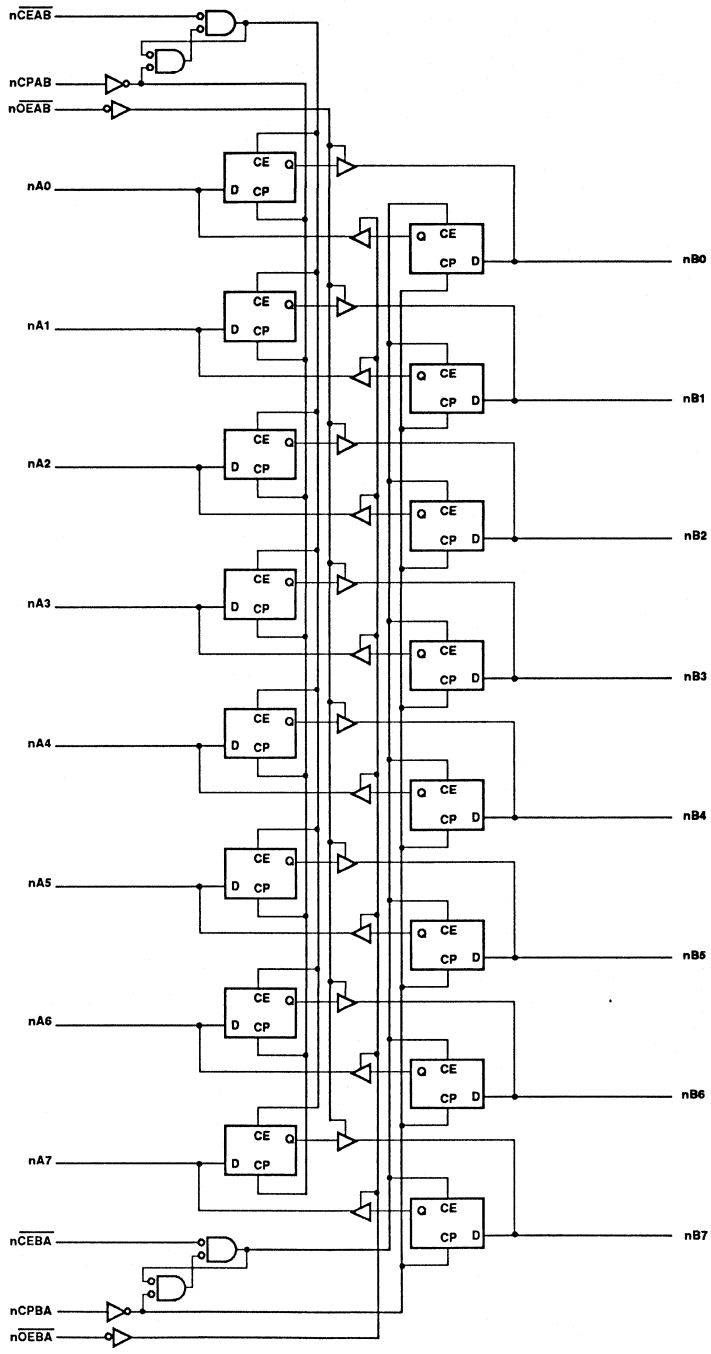
SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		50	100		100	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		48	60		60	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Dual octal registered transceiver, inverting (3-State)

MB2053

FEATURES

- 16-bit inverting registered transceiver
- Multiple V_{CC} and GND pins minimize switching noise
- Independent registers for A and B buses
- AM2953 functional equivalent
- Outputs sink 64mA and source 32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	C_L = 50pF; V_{CC} = 5V	5.7	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

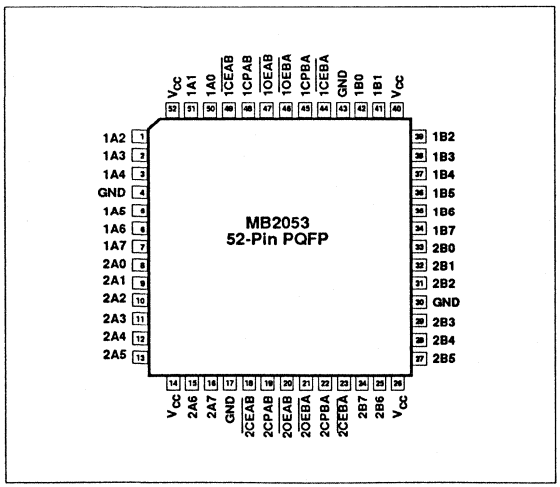
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
52-pin plastic QFP	-40°C to +85°C	MB2053B

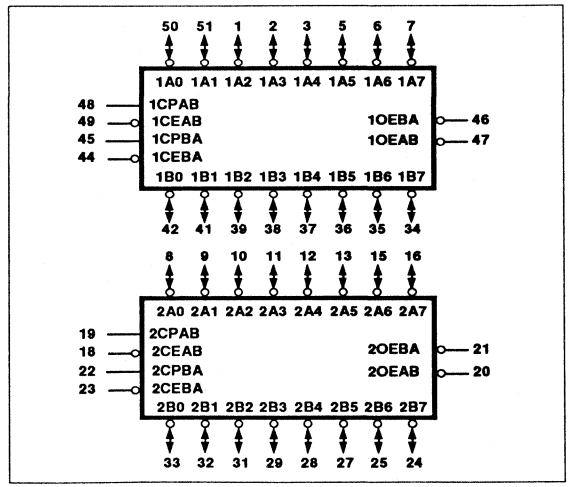
DESCRIPTION

The MB2053 is a dual octal inverting registered transceiver. Two 8-bit registers store data flowing in both directions between two bi-directional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

PIN CONFIGURATION



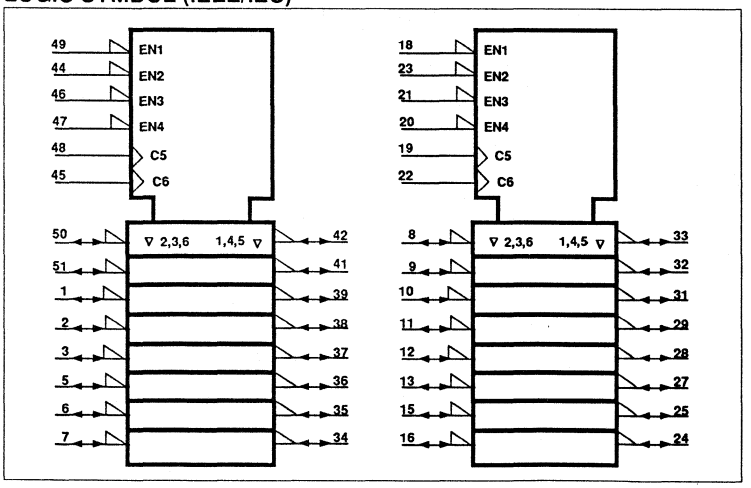
LOGIC SYMBOL



PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1A0 - 1A7, 2A0 - 2A7	50, 51, 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16	Data inputs
1B0 - 1B7, 2B0 - 2B7	42, 41, 39, 38, 37, 36, 35, 34, 33, 32, 31, 29, 28, 27, 25, 24	Data outputs
$1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$	47, 46, 20, 21	Output enables
$1\overline{CEAB}$, $1\overline{CEBA}$, $2\overline{CEAB}$, $2\overline{CEBA}$	49, 44, 18, 23	Clock enable inputs A to B / Clock enable inputs B to A
1CPAB, 1CPBA, 2CPAB, 2CPBA	48, 45, 19, 22	Clock inputs A to B / Clock inputs B to A
GND	4, 17, 30, 43	Ground (0V)
V_{CC}	14, 26, 40, 52	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



Dual octal registered transceiver, inverting (3-State) MB2053

FUNCTION TABLE for Register nAx or nBx

INPUTS			INTERNAL Q	OPERATING MODE
nAx or nBx	nCPXX	$\overline{1CEXX}$		
X	X	H	NC	Hold data
L	↑	L	H	Load data
H	↑	L	L	

H = High voltage level
L = Low voltage level
↑ = Low-to-High transition
X = Don't care
XX = AB or BA
NC = No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL	An or Bn	OPERATING
$\overline{nOEXX}$	Q	OUTPUTS	MODE
H	X	Z	Disable outputs
L	L	H	Enable outputs
L	H	L	

H = High voltage level
L = Low voltage level
X = Don't care
XX = AB or BA

ABSOLUTE MAXIMUM RATINGS[1, 2]

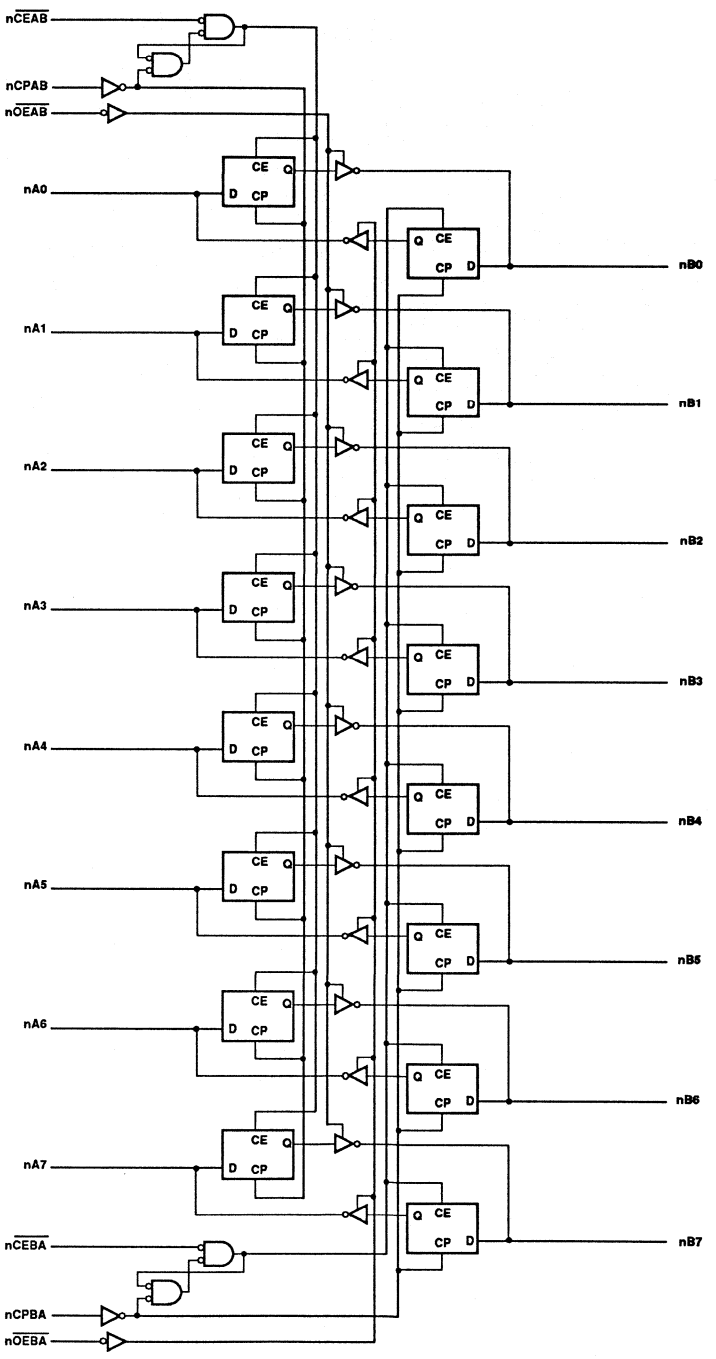
SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
I_{IH} + I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		50	100		100	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		48	60		60	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

16-bit inverting buffer/line driver (3-State) — MB2240

FEATURES

- 16-bit bus interface
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State buffers
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The MB2240 high-performance Bi-CMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2240 device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3-State outputs.

FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nAx	$n\overline{Y}x$
L	L	H
L	H	L
H	X	Z

H = High voltage level
L = Low voltage level
Z = High-impedance "OFF" state

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to $n\overline{Y}x$	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

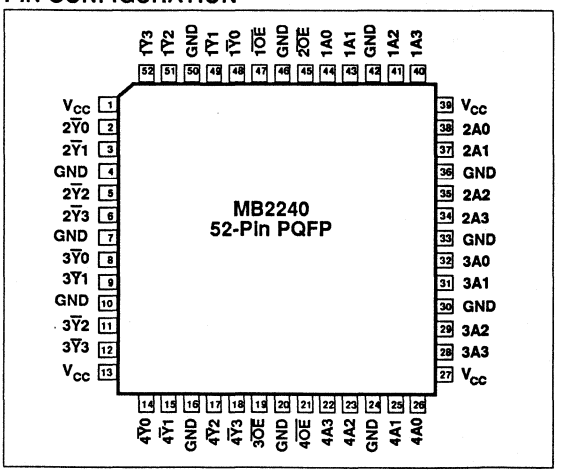
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
52-pin plastic QFP	-40°C to +85°C	MB2240B

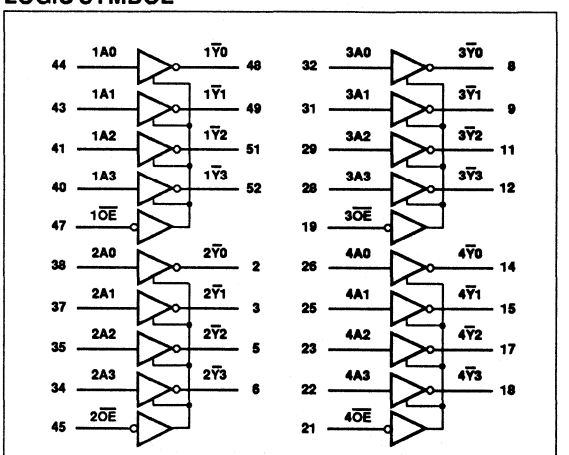
PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1A0 - 1A3, 2A0 - 2A3, 3A0 - 3A3, 4A0 - 4A3	44, 43, 41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	Data inputs
$1\overline{Y}0$ - $1\overline{Y}3$, $2\overline{Y}0$ - $2\overline{Y}3$, $3\overline{Y}0$ - $3\overline{Y}3$, $4\overline{Y}0$ - $4\overline{Y}3$	14, 15, 17, 18, 8, 9, 11, 12, 2, 3, 5, 6, 48, 49, 51, 52	Data outputs
$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	47, 45, 19, 21	Output enables
GND	4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	Ground (0V)
V_{CC}	1, 13, 27, 39	Positive supply voltage

PIN CONFIGURATION

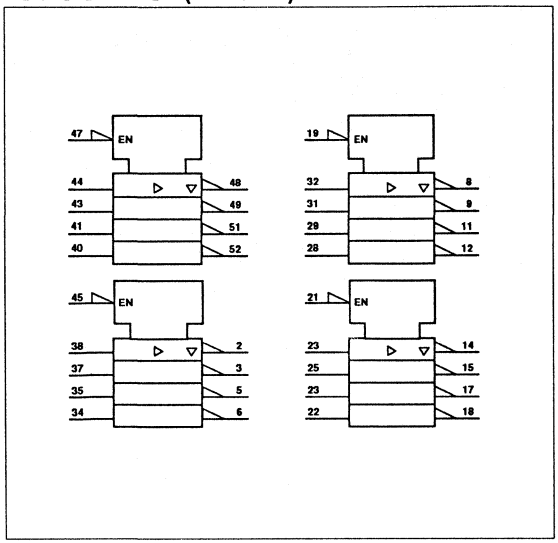


LOGIC SYMBOL



16-bit inverting buffer/line driver (3-State) MB2240

LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		50	100		100	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		48	60		60	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

16-bit buffer/line driver (3-State) MB2241

FEATURES

- 16-bit bus interface
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State buffers
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The MB2241 high-performance Bi-CMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2241 device is a 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, 2OE, $3\overline{OE}$, 4OE), each controlling four of the 3-State outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

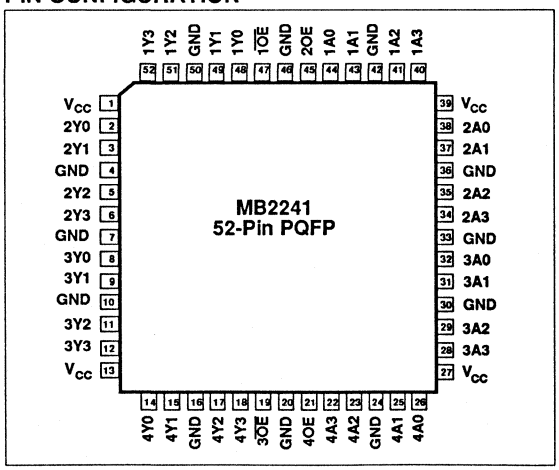
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
52-pin plastic QFP	-40°C to +85°C	MB2241B

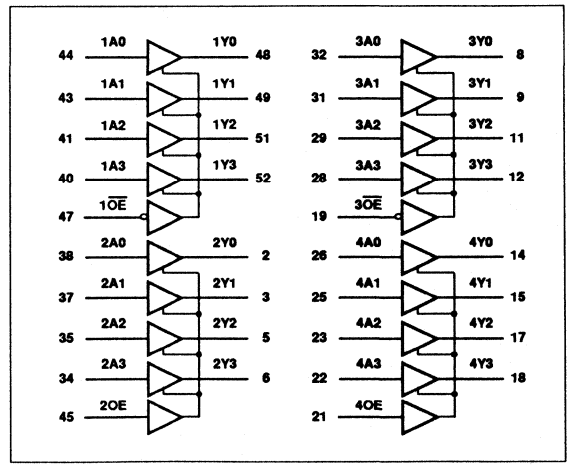
PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1A0 - 1A3, 2A0 - 2A3, 3A0 - 3A3, 4A0 - 4A3	44, 43, 41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	Data inputs
1Y0 - 1Y3, 2Y0 - 2Y3, 3Y0 - 3Y3, 4Y0 - 4Y3	14, 15, 17, 18, 8, 9, 11, 12, 2, 3, 5, 6, 48, 49, 51, 52	Data outputs
$1\overline{OE}$, 2OE, $3\overline{OE}$, 4OE	47, 45, 19, 21	Output enables
GND	4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	Ground (0V)
V_{CC}	1, 13, 27, 39	Positive supply voltage

PIN CONFIGURATION

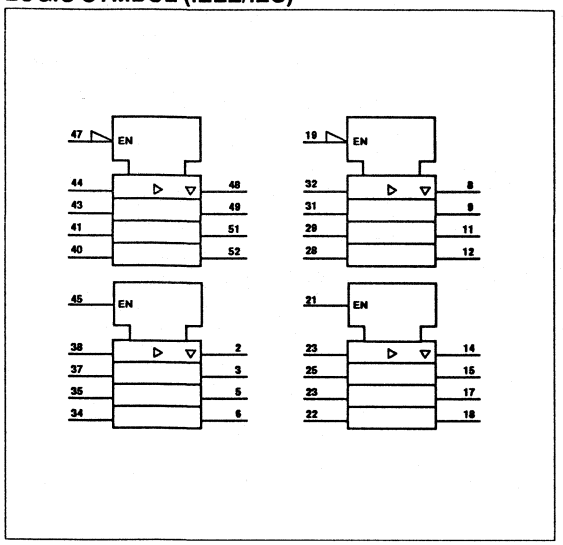


LOGIC SYMBOL



16-bit buffer/line driver (3-State) MB2241

LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS				OUTPUTS	
$1\overline{OE}$ or $3\overline{OE}$	1An or 3An	2OE or 4OE	2An or 4An	1Yn or 3Yn	2Yn or 4Yn
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

H = High voltage level
L = Low voltage level
Z = High-impedance "OFF" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		50	100		100	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		48	60		60	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

16–bit buffer/line driver (3–State) MB2244

FEATURES

- 16–bit bus interface
- Multiple V_{CC} and GND pins minimize switching noise
- 3–State buffers
- Output capability: +64 mA/–32mA
- Latch–up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The MB2244 high–performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2244 device is an 16–bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3–State outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	500	nA

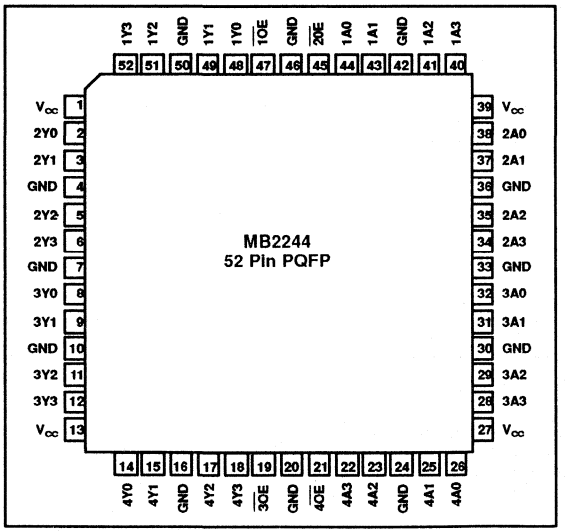
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
52–pin plastic QFP	–40°C to +85°C	MB2244B

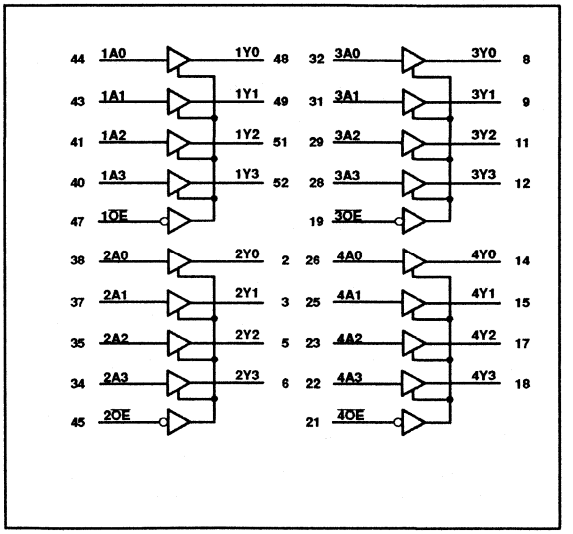
FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nAx	nYx
L	L	L
L	H	H
H	X	Z

PIN CONFIGURATION



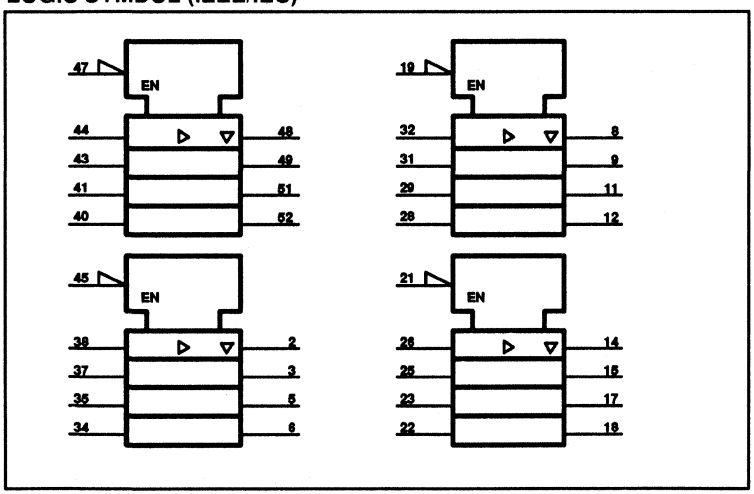
LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
44, 43, 41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	1A0 – 1A3, 2A0 – 2A3, 3A0 – 3A3, 4A0 – 4A3	Data inputs
14, 15, 17, 18, 8, 9, 11, 12, 2, 3, 5, 6, 48, 49, 51, 52	1Y0 – 1Y3, 2Y0 – 2Y3, 3Y0 – 3Y3, 4Y0 – 4Y3	Data outputs
47, 45, 19, 21	$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	Output enables
4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	GND	Ground (0V)
1, 13, 27, 39	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[2]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[2]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1 Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
2 The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		–32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	operating free–air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High–level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low–level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3–State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3–State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_O	Short–circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		50	100		100	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		48	60		60	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		50	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1 Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2 This is the increase in supply current for each input at 3.4V.

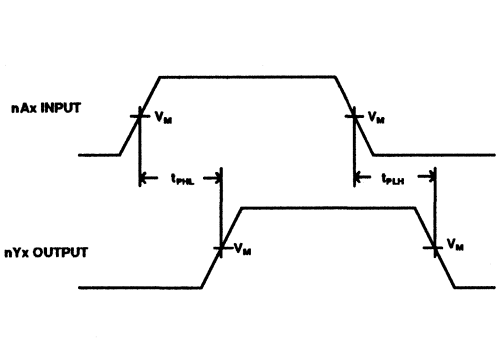
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

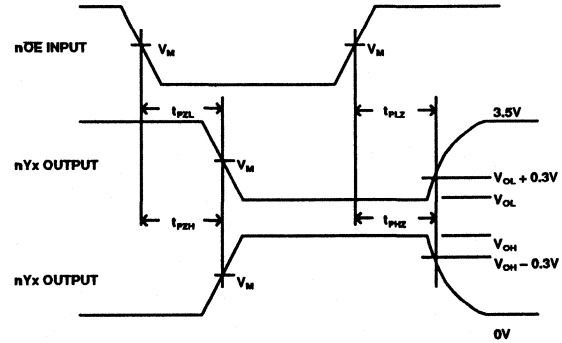
SYMBOL	PARAMETER	WAVEFORM	MB2244					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.0 1.0	2.6 2.9	4.1 4.2	1.0 1.0	4.6 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 2.1	3.1 4.1	4.6 5.6	1.1 2.1	5.1 6.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.1 1.7	4.1 3.7	5.6 5.2	2.1 1.7	6.6 5.7	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

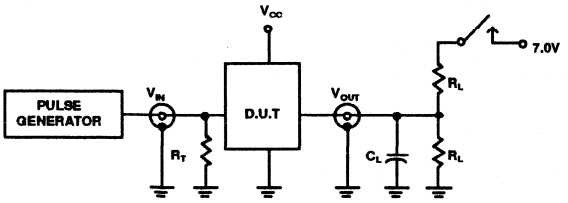


Waveform 1. Waveforms Showing the Input (An) to Output (Yn) Propagation Delays

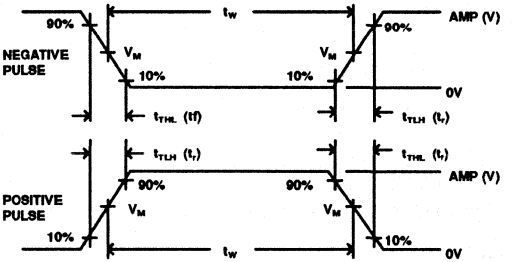


Waveform 2. Waveforms Showing the 3–State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3–State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1Mhz	500ns	2.5ns	2.5ns

Dual octal transceivers with direction pins (3-State) MB2245

FEATURES

- 16-bit bidirectional bus interface
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State buffers
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The MB2245 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2245 device is an dual octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features two Output Enable ($1\overline{OE}$, $2\overline{OE}$) inputs for easy cascading and two Direction (1DIR, 2DIR) inputs for direction control.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$n\overline{OE}$	nDIR	nAx	nBx
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx, or nBx to nAx	C_L = 50pF; V_{CC} = 5V	3.4	ns
$C_{DIR, \overline{OE}}$	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O pin capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

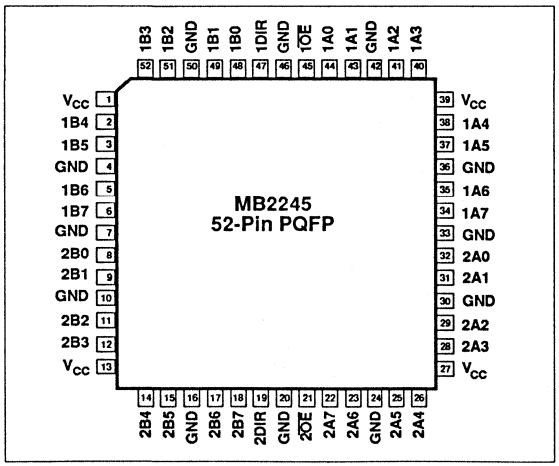
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
52-pin plastic QFP	-40°C to +85°C	MB2245B

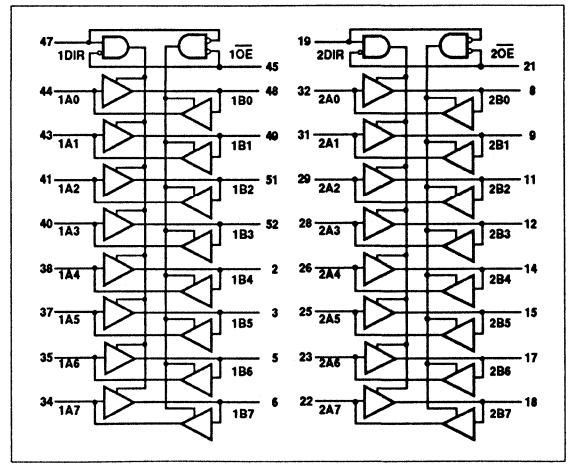
PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1DIR, 2DIR	47, 19	Direction control inputs (Active High)
1A0 - 1A7, 2A0 - 2A7	44, 43, 41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	Data inputs/outputs (A side)
1B0 - 1B7 2B0 - 2B7	48, 49, 51, 52, 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18	Data inputs/outputs (B side)
$1\overline{OE}$, $2\overline{OE}$	45, 21	Output Enable inputs (Active Low)
GND	4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	Ground (0V)
V_{CC}	1, 13, 27, 39	Positive supply voltage

PIN CONFIGURATION

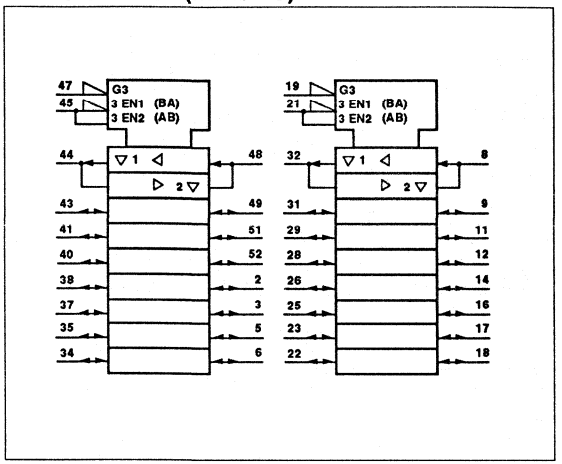


LOGIC SYMBOL



Dual octal transceivers with direction pins (3-State) MB2245

LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
I_{IH} + I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		50	100		100	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		48	60		60	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

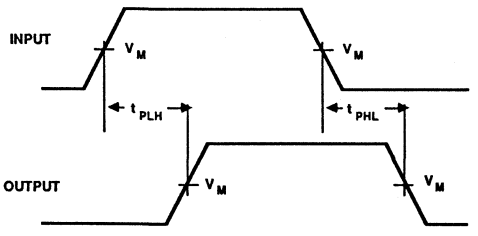
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L= 500Ω

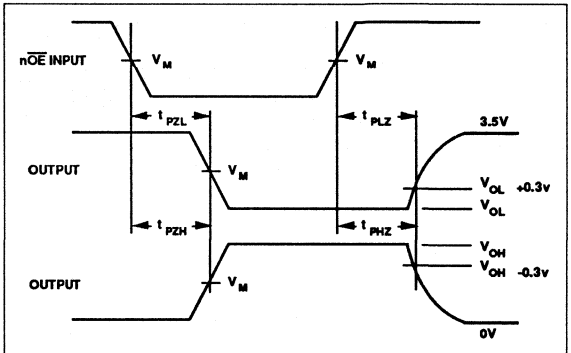
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx, or nBxto nAx	1	1.0 1.0	3.4 3.1	5.0 4.2	1.0 1.0	5.8 4.8	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.3 2.3	3.5 4.8	4.8 6.0	1.3 2.3	5.3 6.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.7 2.3	5.5 4.5	6.5 5.8	2.7 2.3	7.2 6.3	ns

AC WAVEFORMS

(V_M = 1.5V, V_{IN} = GND to 3.0V)

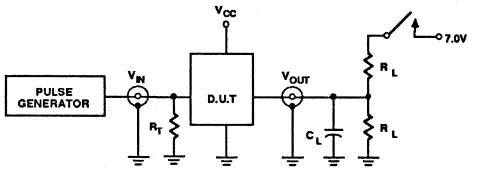


Waveform 1. Waveforms Showing the Input to Output Propagation Delays

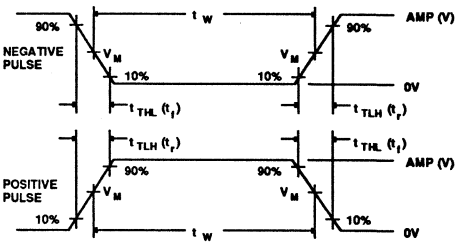


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

Dual octal D-type transparent latch (3-State) MB2373

FEATURES

- 16-bit transparent latch
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State output buffers
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The MB2373 high-performance Bi-CMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2373 device is a dual octal transparent latch coupled to two sets of eight 3-State output buffers. The two sections of the device are controlled independently by Enable (nE) and Output Enable ($n\overline{OE}$) control gates.

The data on each set of D inputs are transferred to the latch outputs when the Latch Enable (nE) input is High. The latch remains transparent to the data inputs while nE is High, and stores the data that is present one setup time before the High-to-Low enable transition.

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	C_L = 50pF; V_{CC} = 5V	4.2	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

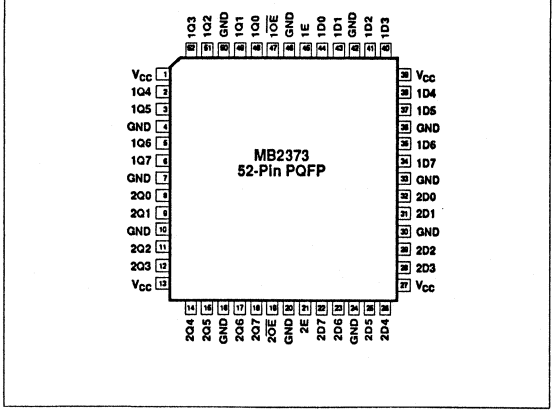
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
52-pin plastic QFP	-40°C to +85°C	MB2373B

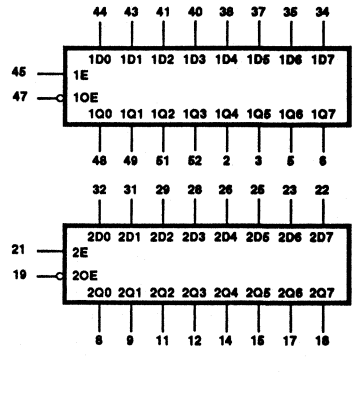
PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1D0 - 1D7, 2D0 - 2D7	44, 43, 41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	Data inputs
1Q0 - 1Q7, 2Q0 - 2Q7	48, 49, 51, 52, 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18	Data outputs (3-State)
$1\overline{OE}$, $2\overline{OE}$	47, 19	Output enable inputs (active Low)
1E, 2E	45, 21	Enable inputs (active High)
GND	4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	Ground (0V)
V_{CC}	1, 13, 27, 39	Positive supply voltage

PIN CONFIGURATION



LOGIC SYMBOL

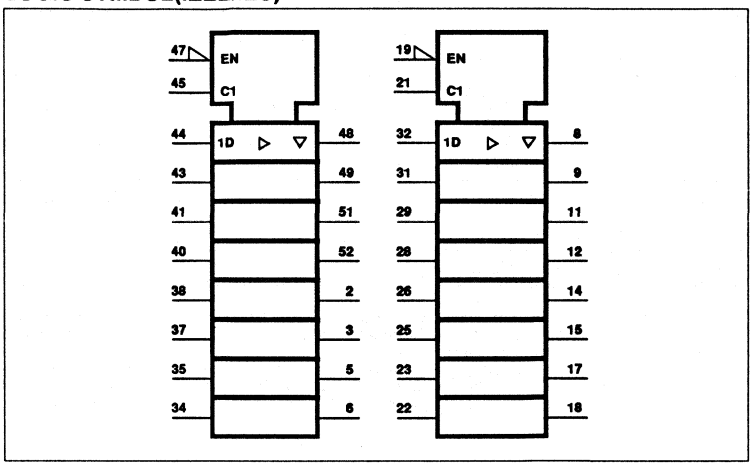


Dual octal D-type transparent latch (3-State) MB2373

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. Each active-Low Output Enable ($\overline{nOE}$) controls a set of eight 3-State buffers independent of the latch operation.

When $\overline{nOE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{nOE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

LOGIC SYMBOL(IEEE/IEC)

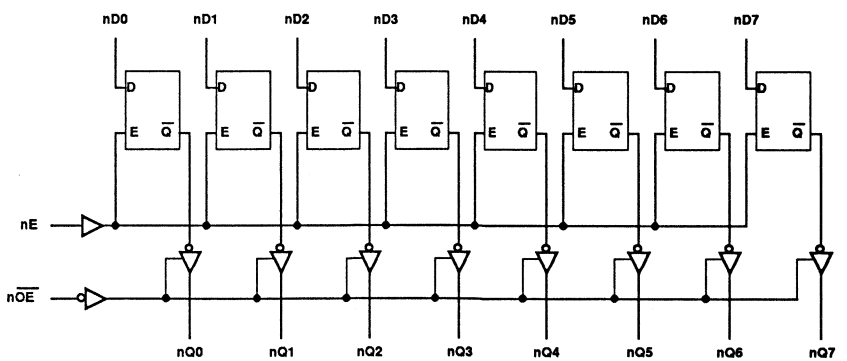


FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{nOE}$	nE	nDx	REGISTER	nQ0 - nQ7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		50	100		100	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		48	60		60	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Dual octal D-type flip-flop; positive-edge trigger (3-State) MB2374

FEATURES

- 16-bit positive edge triggered register
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State output buffers
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The MB2374 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2374 has two 8-bit, edge triggered registers, with each register coupled to eight 3-State output buffers. The two sections of each register are controlled independently by the clock (nCP) and Output Enable ($n\overline{OE}$) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses,

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50pF; V_{CC} = 5V	4.8	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

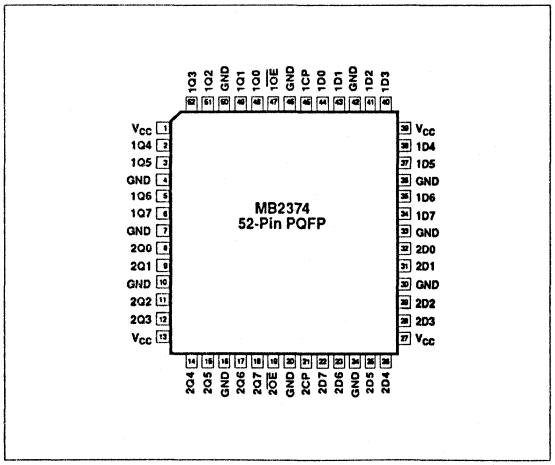
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
52-pin plastic QFP	-40°C to +85°C	MB2374B

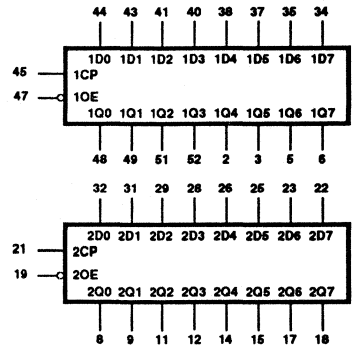
PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1D0 - 1D7, 2D0 - 2D7	44, 43, 41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	Data inputs
1Q0 - 1Q7, 2Q0 - 2Q7	48, 49, 51, 52, 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18	Data outputs (3-State)
$1\overline{OE}$, $2\overline{OE}$	47, 19	Output enable inputs (active Low)
1CP, 2CP	45, 21	Clock pulse inputs (active rising edge)
GND	4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	Ground (0V)
V_{CC}	1, 13, 27, 39	Positive supply voltage

PIN CONFIGURATION



LOGIC SYMBOL

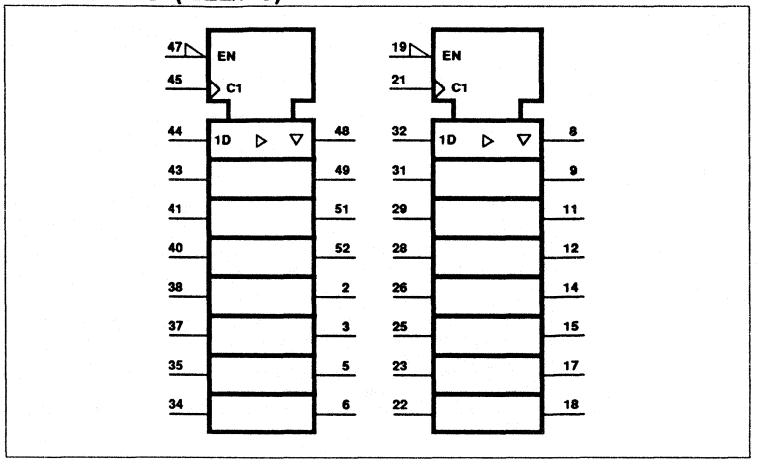


Dual octal D-type flip-flop; positive-edge trigger (3-State) MB2374

MOS memories, or MOS microprocessors. Each active-Low Output Enable ($n\overline{OE}$) controls all eight 3-State buffers for its register independent of the clock operation.

When $n\overline{OE}$ is Low, the stored data appears at the outputs for that register. When $n\overline{OE}$ is High, the outputs for that register are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

LOGIC SYMBOL(IEEE/IEC)

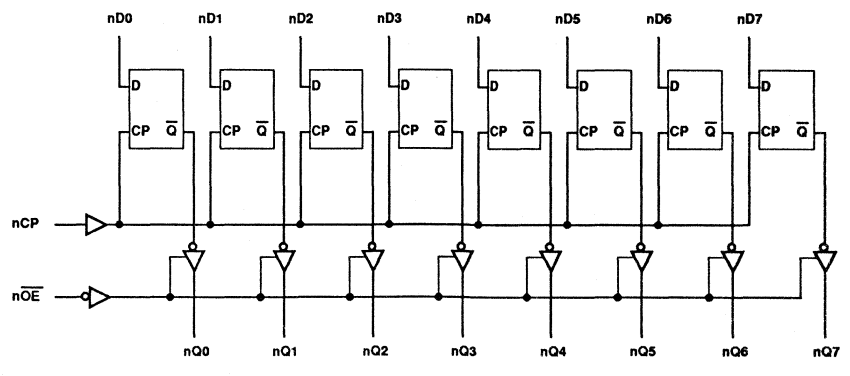


FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nCP	nDx	REGISTER	nQ0 - nQ7	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	↕	X	NC	NC	Hold
H	↕	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = Not a Low-to-High clock transition

LOGIC DIAGRAM



Dual octal D-type flip-flop; positive-edge trigger (3-State) MB2374

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		50	100		100	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		48	60		60	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Dual octal buffer/line drivers (3-State) MB2541

FEATURES

- 16-bit bus interfaces
- Multiple V_{CC} and GND pins minimize switching noise
- Provides ideal interface and increases fan-out of MOS Microprocessors
- Efficient pinout to facilitate PC board layout
- 3-State buffer outputs sink 64mA and source 32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The MB2541 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2541 has two octal buffers that are ideal for driving bus lines. The outputs are all capable of sinking 64mA and sourcing 32mA.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nIx to nYx	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

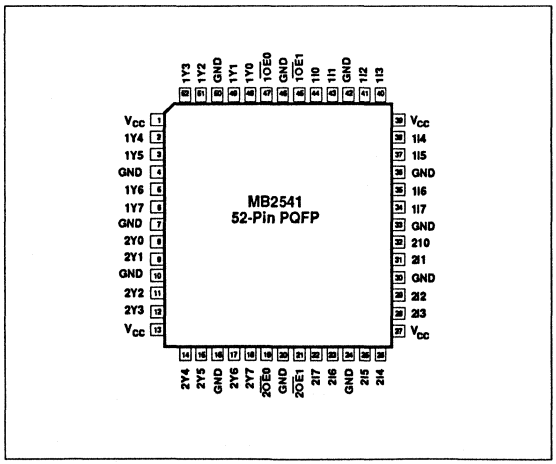
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
52-pin plastic QFP	-40°C to +85°C	MB2541B

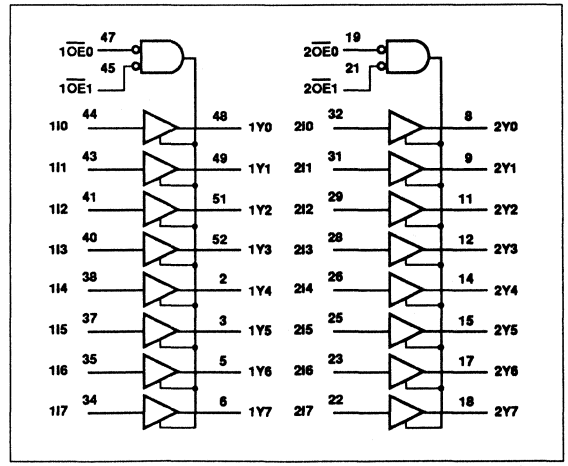
PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1I0 - 1I7, 2I0 - 2I7	44, 43, 41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	Data inputs
1Y0 - 1Y7, 2Y0 - 2Y7	48, 49, 51, 52, 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18	Data outputs (3-State)
$1\overline{OE}0$, $1\overline{OE}1$, $2\overline{OE}0$, $2\overline{OE}1$	47, 45, 19, 21	Output enable inputs (active Low)
GND	4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	Ground (0V)
V_{CC}	1, 13, 27, 39	Positive supply voltage

PIN CONFIGURATION



LOGIC SYMBOL

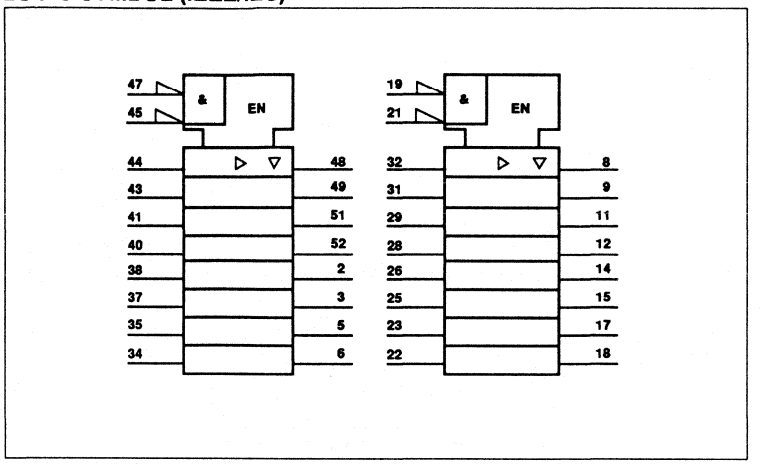


Dual octal buffer/line drivers (3-State) MB2541

FUNCTION TABLE

INPUTS			OUTPUT
$n\overline{OE}0$	$n\overline{OE}1$	nIx	nYx
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		50	100		100	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		48	60		60	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Dual octal latched transceivers with dual enable (3-State) MB2543

FEATURES

- 16-bit dual octal transceiver with D-type latch
- Multiple V_{CC} and GND pins minimize switching noise
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn	C_L = 50pF; V_{CC} = 5V	4.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
52-pin plastic QFP	-40°C to +85°C	MB2543B

DESCRIPTION

The MB2543 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

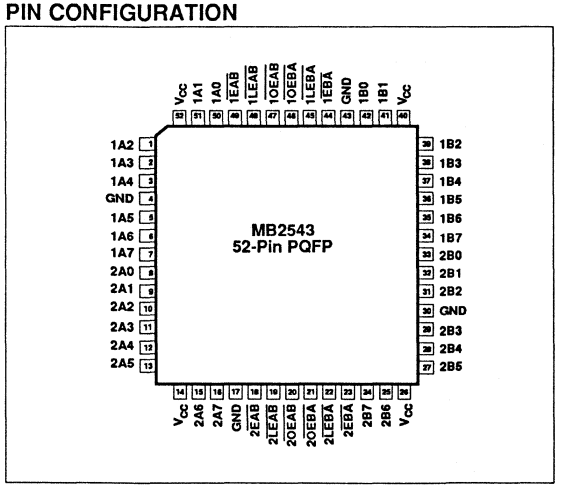
The MB2543 dual octal registered transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable (nLEAB, nLEBA) and Output Enable (nOEAB, nOEBA) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64mA.

FUNCTIONAL DESCRIPTION

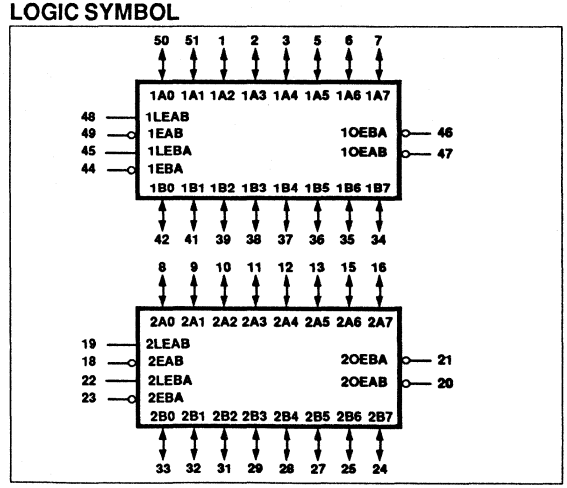
The MB2543 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable (nEAB) input and the A-to-B Latch Enable (nLEAB) input are Low the A-to-B path is transparent. A subsequent Low-to High transition of the nLEAB signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With nEAB and nOEAB both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the nEBA, nLEBA, and nOEBA inputs.

PIN CONFIGURATION



LOGIC SYMBOL

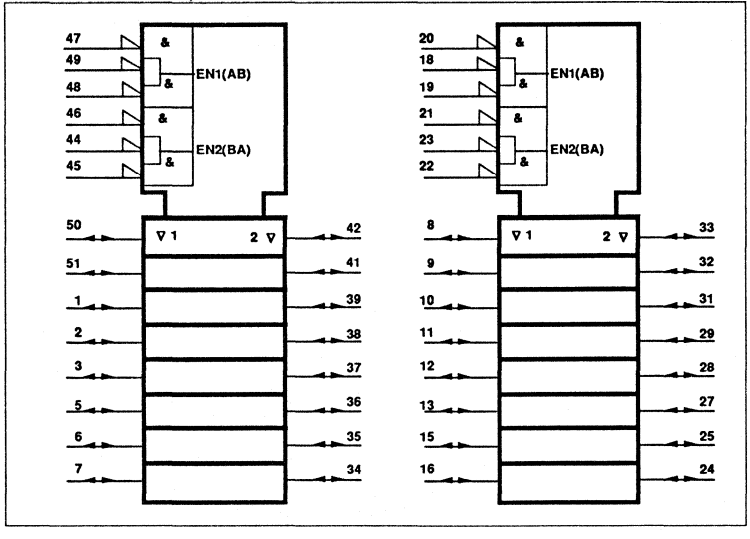


Dual octal latched transceivers with dual enable (3-State) MB2543

PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1A0 - 1A7, 2A0 - 2A7	50, 51, 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16	Data inputs
1B0 - 1B7, 2B0 - 2B7	42, 41, 39, 38, 37, 36, 35, 34, 33, 32, 31, 29, 28, 27, 25, 24	Data outputs
$1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$	47, 46, 20, 21	A to B / B to A Output Enable input (Active Low)
$1\overline{EAB}$, $1\overline{EBA}$, $2\overline{EAB}$, $2\overline{EBA}$	49, 44, 18, 23	A to B / B to A Enable input (Active Low)
1LEAB, 1LEBA, 2LEAB, 2LEBA	48, 45, 19, 22	A to B / B to A Latch Enable input (Active Low)
GND	4, 17, 30, 43	Ground (0V)
V_{CC}	14, 26, 40, 52	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



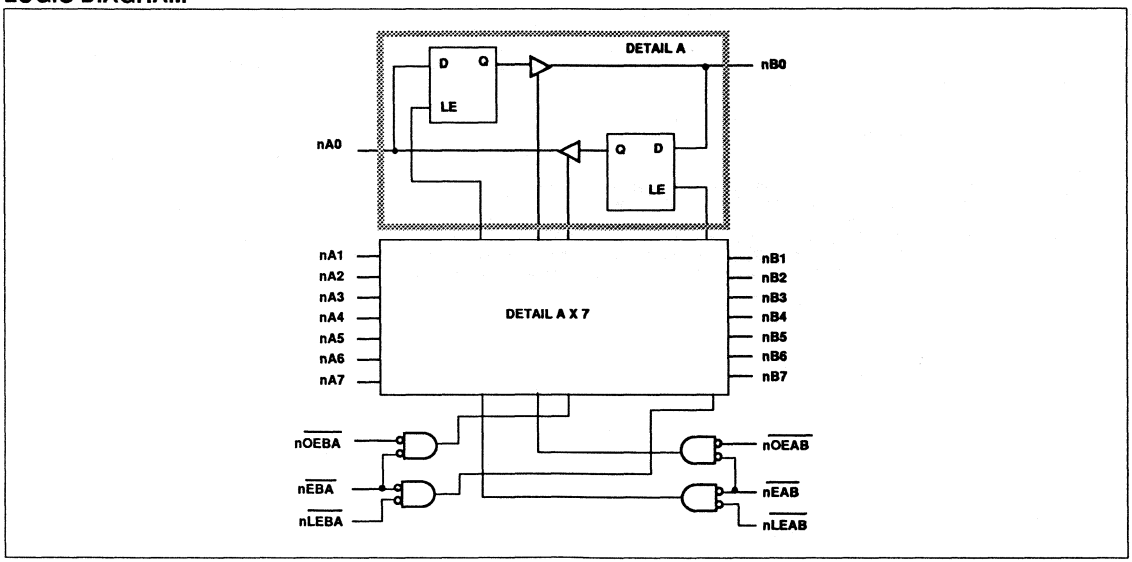
Dual octal latched transceivers with dual enable (3-State) MB2543

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{nOEXX}$	$\overline{nEXX}$	$\overline{nLEXX}$	DATA		
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L	↑	L	h	Z	Disabled + Latch
L	↑	L	l	Z	
L	L	↑	h	H	Latch + Display
L	L	↑	l	L	
L	L	L	H	H	Transparent
L	L	L	L	L	
L	L	H	X	NC	Hold

H= High voltage level
L= Low voltage level
h= High state must be present one setup time before the Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX=AB or BA)
l = Low state must be present one setup time before the Low-to -High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX=AB or BA)
↑ =Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX=AB or BA)
X=Don't care
NC=No change
Z =High impedance "off" state

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
I_{IH} + I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		50	100		100	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		48	60		60	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Dual octal transceiver with dual enable, non-inverting (3-State)

MB2623

FEATURES

- 16-bit bidirectional bus interface
- 3-State buffers
- Multiple V_{CC} and GND pins minimize switching noise
- Output capability: +64 mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The MB2623 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2623 device is a dual octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The MB2623 is designed for asynchronous two-way communication between data buses.

(continued)

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{nOEBA}$	nOEAB	nAx	nBx
L	L	A = B	Inputs
H	H	Inputs	B = A
H	L	Z	Z
L	H	A=B	B=A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx, or nBx to nAx	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{OExx}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O pin capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

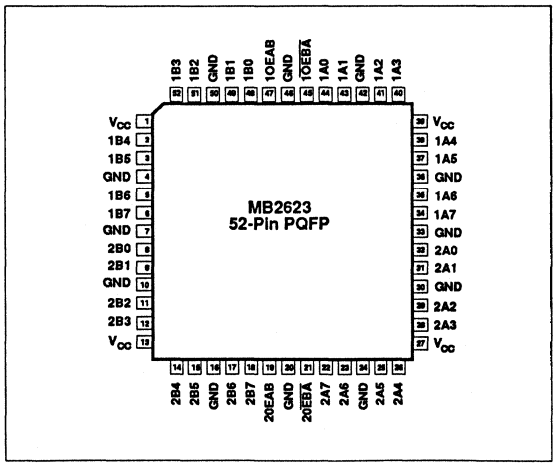
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
52-pin plastic QFP	-40°C to +85°C	MB2623B

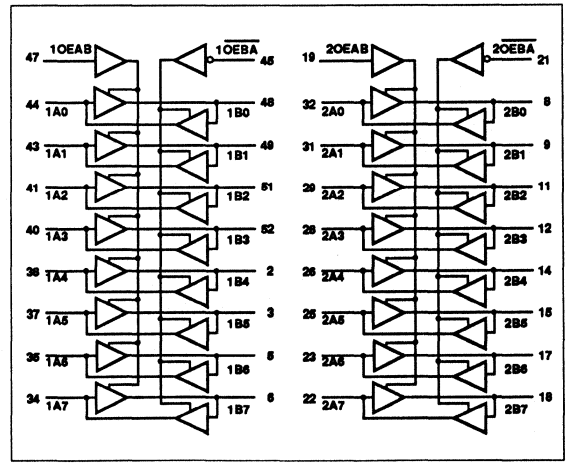
PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1OEAB, 2OEAB	47, 19	Output Enable inputs (Active High)
1A0 - 1A7, 2A0 - 2A7	44, 43, 41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	Data inputs/outputs (A side)
1B0 - 1B7 2B0 - 2B7	48, 49, 51, 52, 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18	Data inputs/outputs (B side)
$1\overline{OEBA}$, $2\overline{OEBA}$	45, 21	Output Enable inputs (Active Low)
GND	4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	Ground (0V)
V_{CC}	1, 13, 27, 39	Positive supply voltage

PIN CONFIGURATION



LOGIC SYMBOL

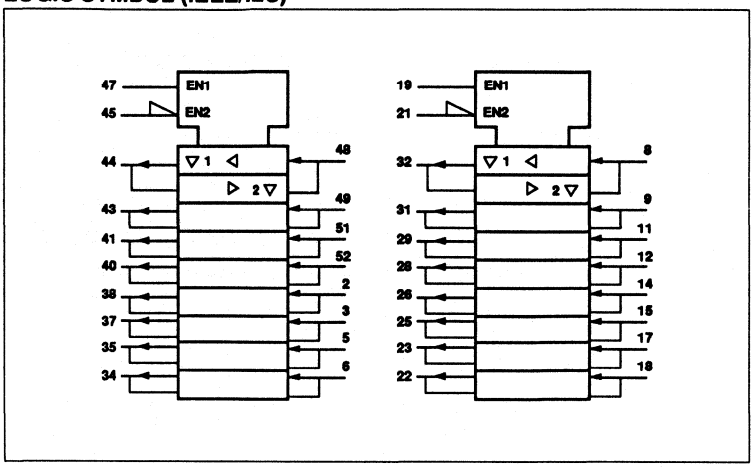


Dual octal transceiver with dual enable, non-inverting (3-State)

MB2623

The control function implementation allows for maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs ($\overline{nOEBA}$ and $\overline{nOEAB}$). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

Dual octal transceiver with dual enable, non-inverting (3-State)

MB2623

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		50	100		100	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		48	60		60	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Dual octal bus transceivers/registers (3-State)

MB2646

FEATURES

- Independent registers for A and B buses
- Multiple V_{CC} and GND pins minimize switching noise
- Multiplexed real-time and stored data
- Outputs sink 64mA and source 32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The MB2646 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2646 dual transceiver/register consists of two sets of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable ($n\overline{OE}$) and Direction (nDIR) pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx, or nBx to nAx	C_L = 50pF; V_{CC} = 5V	4.4	ns
C_{IN}	Input capacitance CP, S, $\overline{OE}$	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

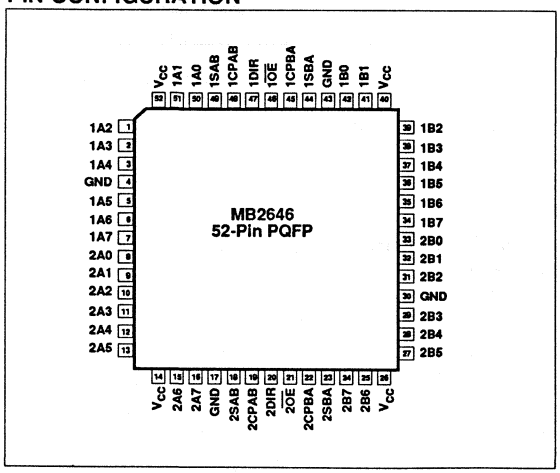
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
52-pin plastic QFP	-40°C to +85°C	MB2646B

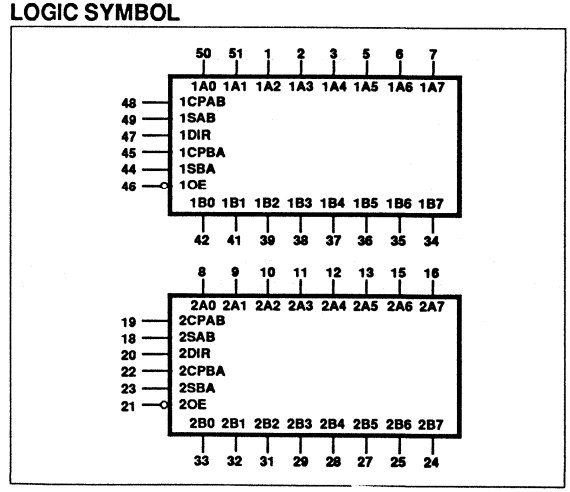
PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1CPAB, 1CPBA, 2CPAB, 2CPBA	48, 45, 19, 22	Clock input A to B / Clock input B to A
1SAB, 1SBA, 2SAB, 2SBA	49, 44, 18, 23	Select input A to B / Select input B to A
1DIR, 2DIR	47, 20	Direction control input
1A0 - 1A7, 2A0 - 2A7	50, 51, 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16	Data inputs/outputs (A side)
1B0 - 1B7 2B0 - 2B7	42, 41, 39, 38, 37, 36, 35, 34, 33, 32, 31, 29, 28, 27, 25, 24	Data inputs/outputs (B side)
$1\overline{OE}$, $2\overline{OE}$	46, 21	Output Enable inputs (Active Low)
GND	4, 17, 30, 43	Ground (0V)
V_{CC}	14, 26, 40, 52	Positive supply voltage

PIN CONFIGURATION



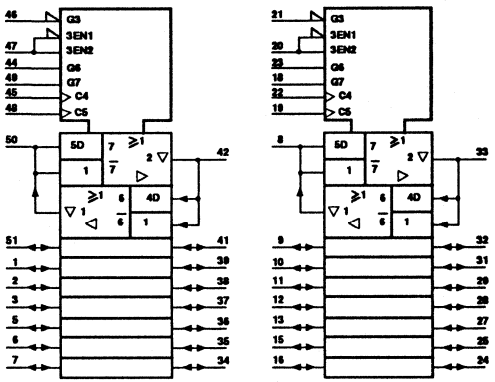
LOGIC SYMBOL



Dual octal bus transceivers/registers (3-State) MB2646

The select (nSAB, nSBA) pins determine whether data is stored or transferred through the device in real-time. The nDIR determines which bus will receive data when the $n\overline{OE}$ is active Low. In the isolation mode ($n\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time. The examples on the next page demonstrate the four fundamental bus management functions that can be performed with the MB2646.

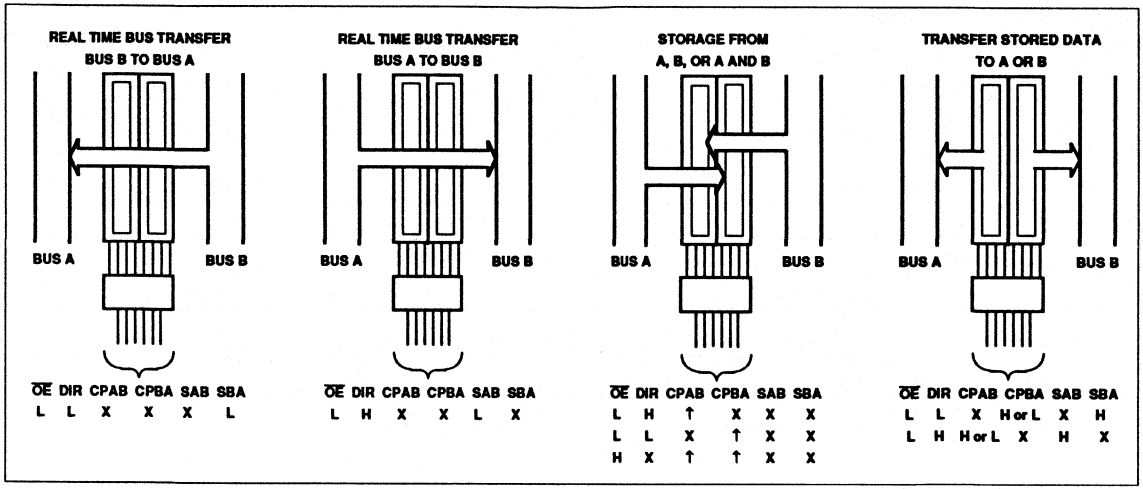
LOGIC SYMBOL (IEEE/IEC)



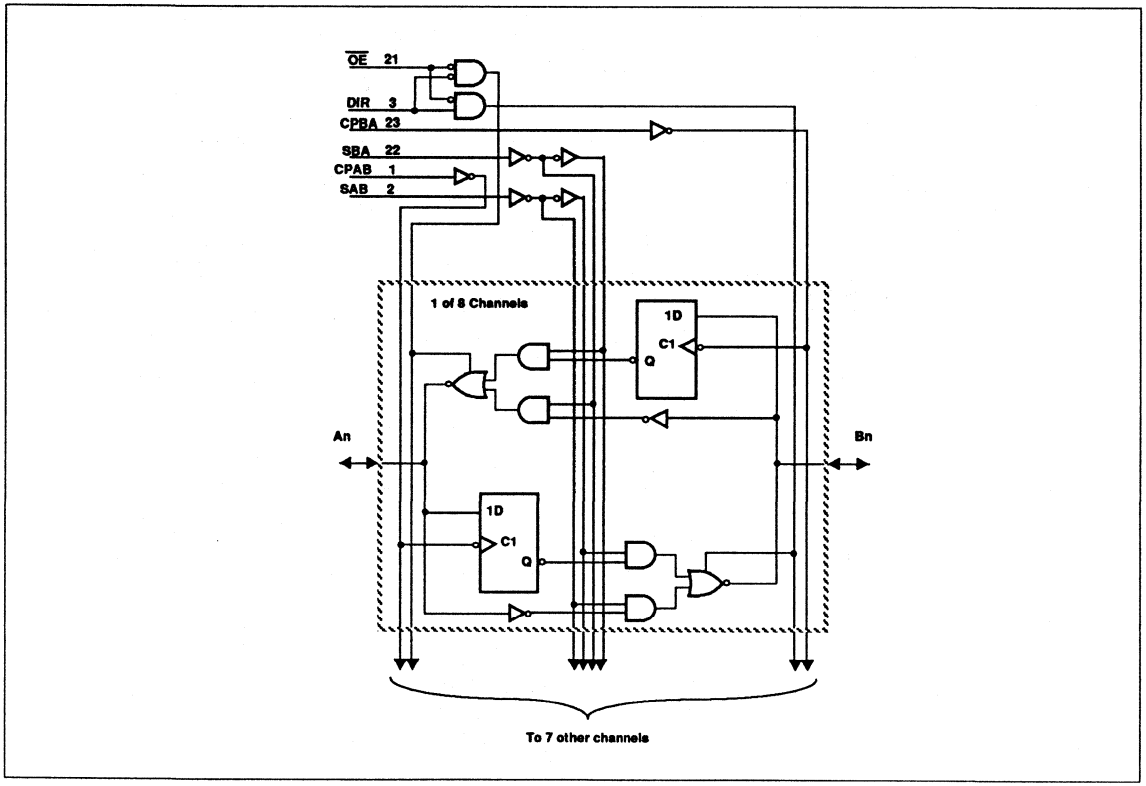
FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA	nA0-nA7	nB0-nB7	
X	X	↑	X	X	X	Input	Unspecified*	Store A, B unspecified*
X	X	X	↑	X	X	Unspecified*	Input	Store B, A unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X			Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real time B data to A bus
L	L	X	H or L	X	H			Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real time A data to B bus
L	H	H or L	X	H	X			Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑= Low-to High clock transition
* = The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to High transition of the clock.



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
I_{IH} + I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		50	100		100	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		48	60		60	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Dual octal transceivers/registers, non-inverting (3-State) MB2652

FEATURES

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 3-State outputs
- Multiple V_{CC} and GND pins minimize switching noise
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The MB2652 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2652 transceiver/ register consists of two sets of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable ($n\overline{OEAB}$, $n\overline{OEBA}$) and Select (nSAB, nSBA) pins are provided for bus management.

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to nAx or nBx	C_L = 50pF; V_{CC} = 5V	5.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

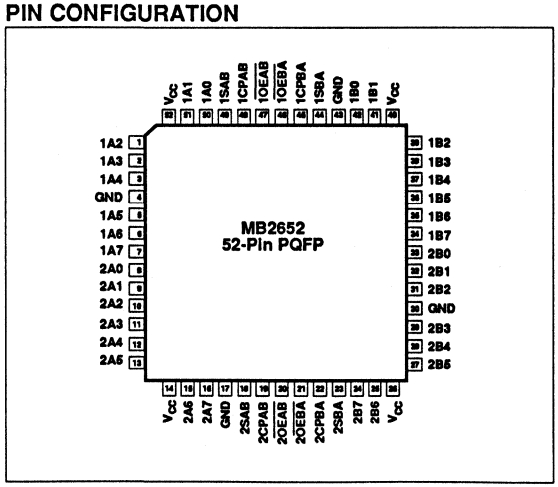
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
52-pin plastic QFP	-40°C to +85°C	MB2652B

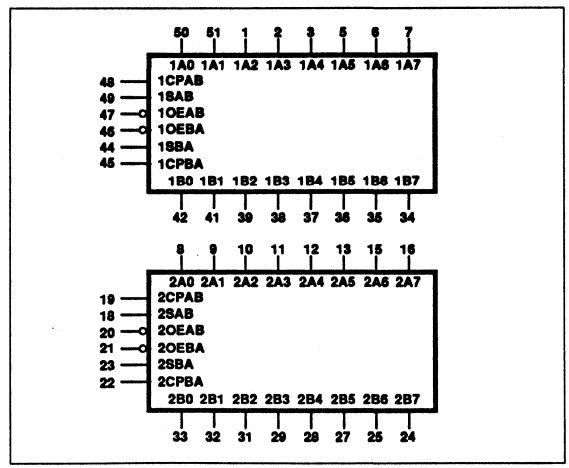
PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1CPAB, 1CPBA, 2CPAB, 2CPBA	48, 45, 19, 22	Clock input A to B / Clock input B to A
1SAB, 1SBA, 2SAB, 2SBA	49, 44, 18, 23	Select input A to B / Select input B to A
1A0 - 1A7, 2A0 - 2A7	50, 51, 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16	Data inputs/outputs (A side)
1B0 - 1B7 2B0 - 2B7	42, 41, 39, 38, 37, 36, 35, 34, 33, 32, 31, 29, 28, 27, 25, 24	Data inputs/outputs (B side)
$1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$	47, 46, 20, 21	Output Enable inputs (Active Low)
GND	4, 17, 30, 43	Ground (0V)
V_{CC}	14, 26, 40, 52	Positive supply voltage

PIN CONFIGURATION



LOGIC SYMBOL



Dual octal transceivers/registers, non-inverting (3-State) MB2652

FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
$n\overline{OEAB}$	$n\overline{OEBA}$	nCPAB	nCPBA	nSAB	nSBA	nAx	nAx	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified output *	Store A, Hold B
H	H	↑	↑	**	X			Store A in both registers
L	X	H or L	↑	X	X	Unspecified output *	Input	Hold A, Store B
L	L	↑	↑	X	**			Store B in both registers
L	L	X	X	X	L	Output	Input	Real time B data to A bus
L	L	X	H or L	X	H			Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real time A data to B bus
H	H	H or L	X	H	X			Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus Stored B data to A bus

H = High voltage level

L= Low voltage level

*= The data output function may be enabled or disabled by various signals at the $n\overline{OEBA}$ and $n\overline{OEAB}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

↑ =Low-to-High clock transition

X = Don't care

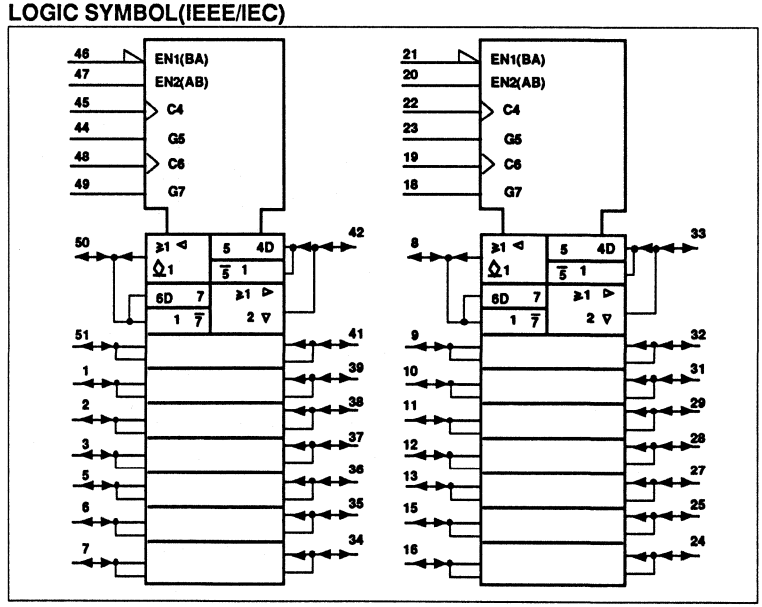
** If Select control = L, then clocks can occur simultaneously. If Select control = H, the clocks must be staggered in order to load both registers.

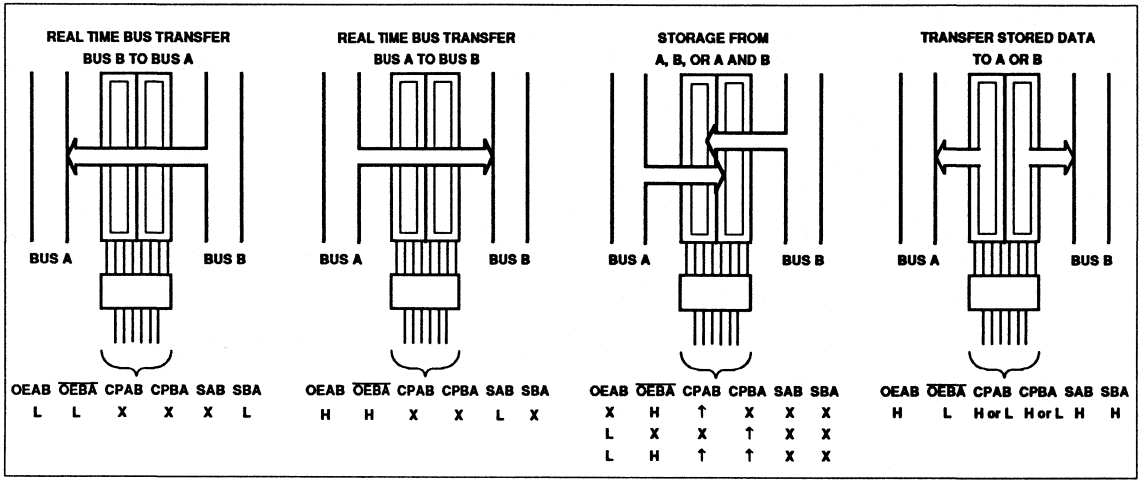
The examples on the next page demonstrate the four fundamental bus-management functions that can be performed with the MB2652.

The select pins determine whether data is stored or transferred through the device in real time.

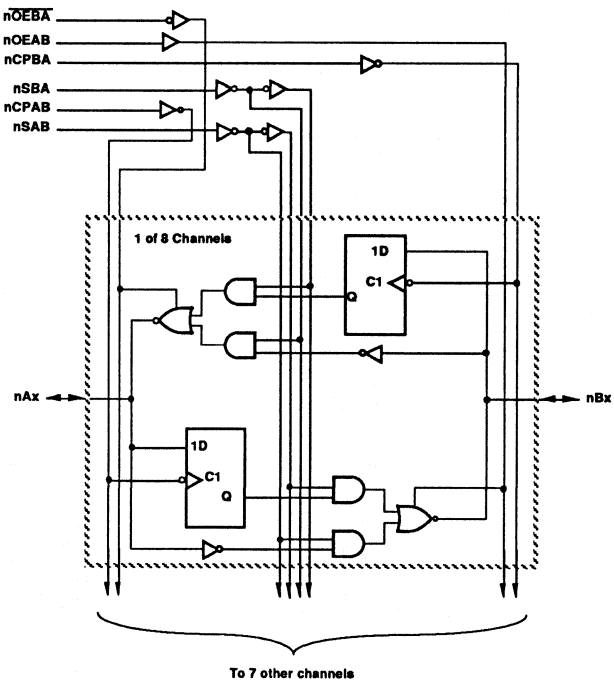
The output enable pins determine the direction of the data flow.

LOGIC SYMBOL(IEEE/IEC)





LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
I_{IH} + I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		50	100		100	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		48	60		60	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Quad octal transceivers with direction pins (3-State) MB4245

FEATURES

- 32-bit bidirectional bus interface
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State buffers
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The MB4245 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB4245 device is an quad octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features four Output Enable ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$) inputs for easy cascading and four Direction (1DIR, 2DIR, 3DIR, 4DIR) inputs for direction control.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx, or nBx to nAx	C_L = 50pF; V_{CC} = 5V	3.4	ns
$C_{DIR, \overline{OE}}$	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O pin capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

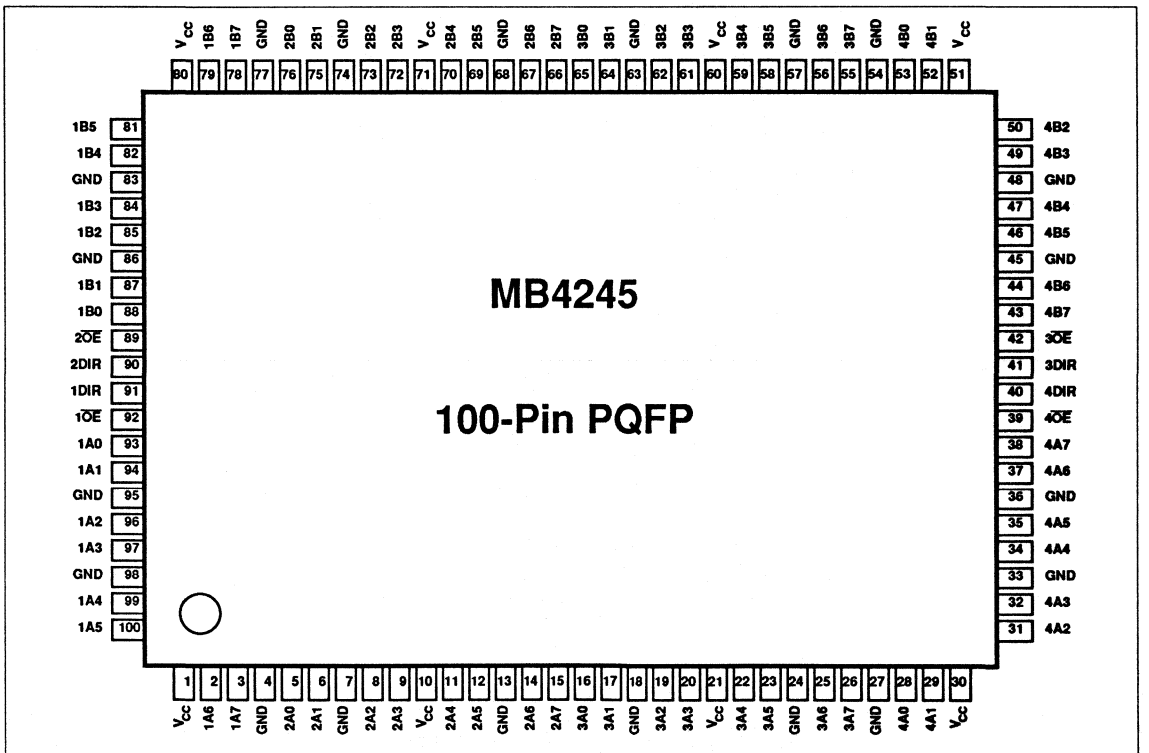
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
100-pin plastic QFP	-40°C to +85°C	MB4245B

FUNCTION TABLE

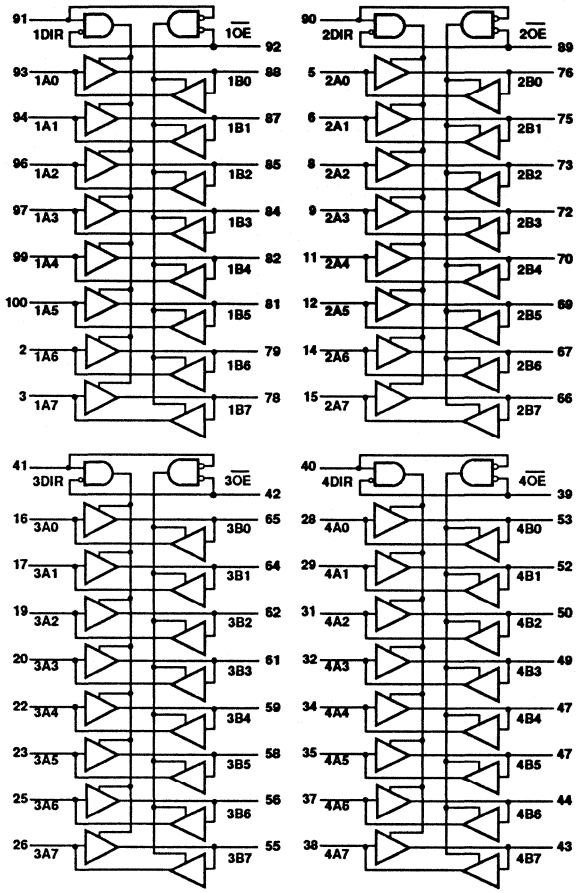
INPUTS		INPUTS/OUTPUTS	
$n\overline{OE}$	nDIR	nAx	nBx
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

PIN CONFIGURATION



Quad octal transceivers with direction pins (3-State) MB4245

LOGIC SYMBOL

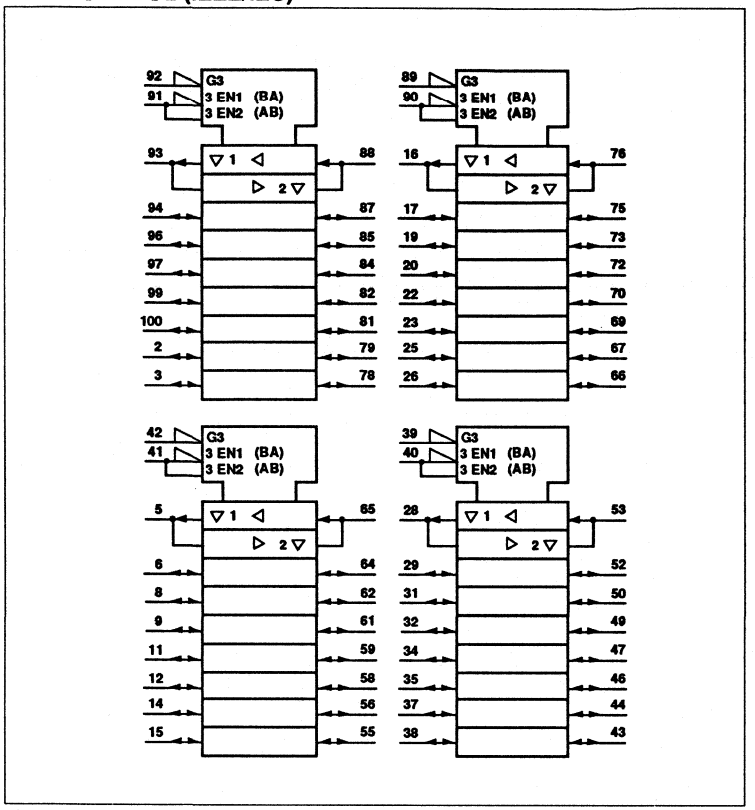


PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1DIR, 2DIR, 3DIR, 4DIR	91, 90, 41, 40	Direction control inputs (Active High)
1A0 - 1A7, 2A0 - 2A7, 3A0 - 3A7, 4A0 - 4A7	93, 94, 96, 97, 99, 100, 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 16, 17, 19, 20, 22, 23, 25, 26, 28, 29, 31, 32, 34, 35, 37, 38	Data inputs/outputs (A side)
1B0 - 1B7, 2B0 - 2B7, 3B0 - 3B7, 4B0 - 4B7,	88, 87, 85, 84, 82, 81, 79, 78, 76, 75, 73, 72, 70, 69, 67, 66, 65, 64, 62, 61, 59, 58, 56, 55, 53, 52, 50, 49, 47, 46, 44, 43	Data inputs/outputs (B side)
$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	92, 89, 42, 40	Output Enable inputs (Active Low)
GND	4, 7, 13, 18, 24, 27, 33, 36, 45, 48, 54, 57, 63, 68, 74, 77, 83, 86, 65, 68	Ground (0V)
V_{CC}	1, 10, 21, 30, 51, 60, 71, 80	Positive supply voltage

Quad octal transceivers with direction pins (3-State) MB4245

LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		50	100		100	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		96	120		120	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Section 6
Application Notes

INDEX

SPICE support for 74ABT/MB2XXX AN230

Signetics' Standard Products Group has been a leader in providing SPICE support to customers. As system operating frequencies go higher, checking signal integrity of digital systems is emerging as an essential design criterion. At higher frequencies, signals are no longer just digital but are analog signals. Also, as combinations of logic products such as discrete logic, PLDs, ASICs, gate arrays and FPGAs are being used together interfacing with CPUs and memories, it is getting more difficult to have tight timing control, clean interface signals and enough tolerance for interface skewing. In designing high frequency digital systems, it is necessary to check for ground bounce, set-up and hold-time violations, reflections, minimum pulse-width violation, signal race conditions, metastability problems, interfacing too long and too short critical paths, skewing between devices or cells and so forth.

The modeling of the inputs, outputs and packages of ICs has been the most challenging task when simulating a whole board with SPICE. Since SPICE is an analog simulation program using numerical analysis methods, it requires high computing power and memory size to have reasonable accuracy and/or required simulation time. However, such a SPICE simulation could save time and money in designing any type of high frequency digital system.

Signetics has been providing customers (on a worldwide basis) with SPICE models of the input, output circuitry and packages of 74F, 74LS/S, ECL, 74AC11K, 74ABT, MB2xxx and FB+ products free of charge. Many system design engineers and incoming inspection engineers have been accustomed to Signetics' excellent SPICE customer support program. We encourage all system designers to do SPICE simulations of critical areas for their prototype designs. By contacting Signetics' SPG marketing in Sunnyvale California, USA, they can get the necessary model files of Signetics' 74ABT and MB2xxx family products.

The SPICE manual provides CMOS and bipolar transistor models, diode models, resistor models, inductances and capacitances for each pin of various packages, input and output circuit diagrams and PSPICE netfiles of the equivalent circuits. All device models are Berkeley 3 SPICE models. As an example, the following information is needed for 74ABT543 and was extracted from Signetics' ABT SPICE manual:

A. Device models
   - a.1. NMOS & PMOS models (the best and the worst case models are also available).
   - a.2. Bipolar transistor models.
   - a.3. Resistor models.
   - a.4. Diode models.

B. Self inductance and capacitance table for 24-pin DIP packages (other package models are also available).

C. Whole package inductance values for 24-pin DIP packages including mutual inductance (other package models are also available).

D. Input and output circuit diagram.

E. An example of the PSPICE netfile of the circuit diagram in (D).

A. Device models.

a.1.NMOS and PMOS nominal transistor models (we provide the worst and the best case models as well).

```
*********************************************************************
*    For better accuracy in fitting narrow-channel transistors,     *
*    the parameter WD was extracted to account for the deviation    *
*    of the actual channel width from the drawn dimensions.         *
*    This parameter is not a standard SPICE level 3 parameter.      *
*    If you want to have a similar accuracy with standard SPICE,    *
*    you will need to adjust transistor widths before simulation    *
*    according to the following formula:                            *
*    W(input to simulator) = Wdrawn - 2*WD, where WD is given       *
*    below for the nominal , fast, and slow cases.                  *
*********************************************************************
*                  NOMINAL N-CHANNEL TRANSISTOR                     *
*                                                                   *
* NOTE: WD=0.037E-6; before simulation, transistor widths need to   *
*       be adjusted: W = Wdrawn - 2*WD = W - 0.074E-6                *
*       Set default L=1.0E-6.  For ABT set default L=1.2E-6          *
*********************************************************************
.MODEL MHS4NEN NMOS
+ LEVEL=3
+ TOX=20E-9
+ UO=436.3
+ VTO=.64
+ NFS=1.09E12
+ NSUB=5.512E16
+ VMAX=150100
*+ RS=24.0
```

```
*+ RD=24.0
+ RSH=240
+ XJ=0.20E-6
+ LD=0.0
+ DELTA=0.0
+ THETA=2.45E-2
+ ETA=.125
+ KAPPA=20E-18
+ PB=.802
+ CJ=5.99E-4
+ MJ=.31
+ CJSW=1.03E-10
+ MJSW=0.2
+ CGDO=3.19E-10
+ CGSO=3.19E-10
*********************************************************************
*                   NOMINAL P-CHANNEL TRANSISTOR                    *
*                                                                   *
* NOTE: WD=0.351E-6; before simulation, transistor widths need to   *
*       be adjusted: Wdrawn = W - 2*WD = W - 0.702E-6                *
*       Set default L=1.0E-6.  For ABT set default L=1.2E-6          *
*********************************************************************
.MODEL MHS4PEN PMOS
+ LEVEL=3
+ TOX=20E-9
+ UO=144.6
+ VTO=-0.75
+ NFS=1E11
+ NSUB=5.504E16
+ VMAX=152100
*+ RS=100.7
*+ RD=100.7
+ RSH=1000
+ XJ=0.225E-6
+ LD=0.166E-6
+ DELTA=.155
+ THETA=6.24E-2
+ ETA=.071
+ KAPPA=20E-18
+ PB=.470
+ CJ=3.68E-4
+ MJ=.213
+ CJSW=1.76E-10
+ MJSW=.33
+ CGDO=3.40E-10
+ CGSO=3.40E-10
```

a.2. Bipolar Transistor models.

```
.MODEL  ESDdriver  NPN  IS= 3.50E-16  BF= 1.24E+02  VAF= 1.13E+01
+  IKF= 9.75E-02
+  BR= 7.12E+00  VAR= 1.63E+00  IKR= 8.17E-03  RB= 2.16E+02  IRB= 1.56E-04
+  RBM= 8.56E-02  RE= 9.69E-02  RC= 7.85E+00  XTB= 1.50E+00  EG= 1.23E+00
+  XTI= 2.14E+00  CJE= 5.59E-13  VJE= 9.53E-01  MJE= 4.67E-01  TF= 4.03E-12
+  CJC= 3.51E-13  VJC= 8.35E-01  MJC= 2.93E-01  TR= 2.93E-10  CJS= 1.91E-13
+  VJS= 6.96E-01  MJS= 4.02E-01
*
*
.MODEL  ESDdriver1  NPN  IS= 3.50E-17  BF= 1.24E+02  VAF= 1.13E+01
+  IKF= 9.75E-03
+  BR= 7.09E+00  VAR= 1.63E+00  IKR= 8.17E-04  RB= 2.16E+03  IRB= 1.56E-05
+  RBM= 8.56E-01  RE= 9.69E-01  RC= 7.85E+01  XTB= 1.50E+00  EG= 1.23E+00
+  XTI= 2.14E+00  CJE= 5.59E-14  VJE= 9.53E-01  MJE= 4.67E-01  TF= 4.03E-12
+  CJC= 3.56E-14  VJC= 8.35E-01  MJC= 2.93E-01  TR= 2.97E-10  CJS= 1.91E-14
+  VJS= 6.96E-01  MJS= 4.02E-01
```

```
*
*
..MODEL  BN10  NPN  IS= 2.59E-17  BF= 1.10E+02  VAF= 2.72E+01  IKF= 1.71E-02
+  BR= 1.55E+00  VAR= 3.42E+00  IKR= 1.00E-03  RB= 7.58E+02  IRB= 1.56E-04
+  RBM= 2.37E+01  RE= 1.09E+00  RC= 4.43E+01  XTB= 1.50E+00  EG= 1.23E+00
+  XTI= 2.14E+00  CJE= 1.02E-13  VJE= 9.86E-01  MJE= 4.42E-01  TF= 5.33E-12
+  CJC= 4.10E-14  VJC= 8.21E-01  MJC= 3.62E-01  TR= 1.73E-09  CJS= 5.86E-14
+  VJS= 7.12E-01  MJS= 3.91E-01
*
*
.SUBCKT  BNO60  1 2 3 4
QN   1 2 3 4 MTRN
DSCH   2 1 MSCH
.MODEL  MTRN  NPN  IS= 1.30E-16  BF= 1.10E+02  VAF= 2.72E+01  IKF= 9.44E-02
+  BR= 1.63E+00  VAR= 3.42E+00  IKR= 5.62E-03  RB= 1.21E+02  IRB= 8.57E-04
+  RBM= 4.23E+00  RE= 2.18E-01  RC= 7.00E+00  XTB= 1.50E+00  EG= 1.23E+00
+  XTI= 2.14E+00  CJE= 5.13E-13  VJE= 9.86E-01  MJE= 4.42E-01  TF= 5.33E-12
+  CJC= 1.96E-13  VJC= 8.21E-01  MJC= 3.62E-01  TR= 1.65E-09  CJS= 3.12E-13
+  VJS= 7.12E-01  MJS= 3.91E-01
.MODEL MSCH D(IS= 4.28E-13  RS=0.0  N= 1.04E+00  CJO= 1.13E-14  VJ= 7.86E-01
+       M= 5.00E-01  EG= 8.00E-01  XTI= 4.00E+00)
.ENDS BNO60
*
*
.SUBCKT  BNO240  1 2 3 4
QN   1 2 3 4 MTRN
DSCH   2 1 MSCH
.MODEL  MTRN  NPN  IS= 5.22E-16  BF= 1.10E+02  VAF= 2.72E+01  IKF= 3.77E-01
+  BR= 1.63E+00  VAR= 3.42E+00  IKR= 2.24E-02  RB= 3.04E+01  IRB= 3.43E-03
+  RBM= 1.05E+00  RE= 5.47E-02  RC= 1.96E+00  XTB= 1.50E+00  EG= 1.23E+00
+  XTI= 2.14E+00  CJE= 2.05E-12  VJE= 9.86E-01  MJE= 4.42E-01  TF= 5.33E-12
+  CJC= 7.85E-13  VJC= 8.21E-01  MJC= 3.62E-01  TR= 1.65E-09  CJS= 1.24E-12
+  VJS= 7.12E-01  MJS= 3.91E-01
.MODEL MSCH D(IS= 1.17E-12  RS=0.0  N= 1.04E+00  CJO= 4.43E-14  VJ= 7.86E-01
+       M= 5.00E-01  EG= 8.00E-01  XTI= 4.00E+00)
.ENDS BNO240
*
*
a.3. Resistor models.

.SUBCKT ESDbn 1 2 3 PAR HRES RES
R1 1 4 HRES TC= 1.3E-03,  2.0E-06
R2 4 2 HRES TC= 1.3E-03,  2.0E-06
D1 3 4 DSUB RES
.MODEL DSUB D CJO = 3.25E-16 VJ = 6.0E-01  M = 4.0E-01
.ENDS ESDbn
*
*
.SUBCKT ESDsp 1 2 3 PAR HRES RES
R1 1 4 HRES TC= 1.9E-04,  7.7E-06
R2 4 2 HRES TC= 1.9E-04,  7.7E-06
D1 4 3 DSUB RES
.MODEL DSUB D CJO = 3.6E-18 VJ = .835  M = .293
.ENDS ESDsp
*
*
*(** on ESDsp the third node is the n side of the isolation junction and
* should be connected to the input of the ESD macro.**)
*
*
.SUBCKT r250w8 1 2 3 PAR HRES RES
R1 1 4 HRES TC= 1.38E-4,  1.42E-6
R2 4 2 HRES TC= 1.38E-4,  1.42E-6
D1 3 4 DSUB RES
.MODEL DSUB D CJO = 1.2E-17 VJ = 1000  M = 0
```

```
.ENDS r250w8
*
*
a.4. Diode models.

*.SUBCKT  hvds240  1 2 3
DDIO 1 2 MDIO
DSUB 3 2 MSUB OFF
.MODEL MDIO D(IS= 3.42E-12  RS= 2.01E+00  N= 1.00E+00  CJO= 1.06E-13
+       VJ= 7.86E-01
+       M= 4.99E-01  EG= 8.00E-01  XTI= 4.00E+00)
.MODEL MSUB D(CJO= 1.40E-13  VJ= 6.96E-01  M= 4.02E-01)
.ENDS hvds240

*
.SUBCKT  huds5x8  1 2 3
DDIO 1 2 MDIO
DSUB 3 2 MSUB OFF
.MODEL MDIO D(IS= 2.57E-13  RS= 5.54E+01  N= 9.99E-01  CJO= 1.13E-14
+       VJ= 7.86E-01
+       M= 4.99E-01  EG= 8.00E-01  XTI= 4.00E+00)
.MODEL MSUB D(CJO= 3.18E-14  VJ= 7.00E-01  M= 3.96E-01)
.ENDS huds5x8
*
*
.SUBCKT  huds24x4  1 2 3
DDIO 1 2 MDIO
DSUB 3 2 MSUB OFF
.MODEL MDIO D(IS= 1.14E-12  RS= 8.29E+00  N= 9.99E-01  CJO= 5.03E-14
+       VJ= 7.86E-01
+       M= 4.99E-01  EG= 8.00E-01  XTI= 4.00E+00)
.MODEL MSUB D(CJO= 6.10E-14  VJ= 7.00E-01  M= 3.96E-01)
.ENDS huds24x4
```

B. Self Inductance and capacitance table of 24 pin DIP package.

Pin #s	Self inductance	Capacitance
1	15.10nH	1.86pF
2	12.20	1.70
3	9.54	1.29
4	7.44	0.95
5	5.31	0.61
6	3.73	0.43
7	3.41	0.43
8	4.66	0.61
9	6.95	0.95
10	8.96	1.29
11	11.70	1.70
12	14.50	1.86
13	14.50	1.86
14	11.70	1.70
15	8.96	1.29
16	6.95	0.95
17	4.66	0.61
18	3.41	0.43
19	3.27	0.43
20	5.31	0.61
21	7.44	0.95
22	9.58	1.29
23	12.20	1.70
24	15.10	1.86

C. WholePackage inductance values of 24 pin DIP including mutual inductances information.

```
TITLE @ DIP24 lead frame
TERMINALS       48 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22 A23 A24 B1
B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20 B21 B22 B23 B24
LEAD    24              25      1               26      2               27      3               28
 4              5       29              6       30              7       31              8       32
33      9               34      10              35      11              36      12              37
13              38      14              39      15              40      16              41      17
42      18              43      19              44      20              45      21              46
22              47      23              48      24
$
$ Inductance Matrix
        1.51E-08
$
        7.68E-091.22E-08
$
        4.66E-095.79E-099.54E-09
$
        2.89E-093.33E-094.20E-097.44E-09
$
 -1.56E-09 -1.75E-09 -2.01E-09 -2.55E-089.31E-09
$
 -6.38E-10 -7.27E-10 -8.29E-10 -1.02E-019.41E-093.73E-09
$
        4.99E-11 -2.23E-11 -1.01E-10 -2.17E-10 4.06E-108.21E-103.41E-09
$
        4.43E-103.55E-102.58E-101.39E-103.99E-113.49E-101.18E-094.66E-09
$
 -7.56E-10 -6.43E-10 -5.18E-10 -3.80E-100.82E-10 -1.26E-10 -7.91E-10 -2.04E-09 6.95E-09
$
 -9.86E-10 -8.52E-10 -7.02E-10 -5.42E-130.23E-103.19E-12 -6.18E-10 -1.62E-09   3.69E-098.96E-09
$
 -1.22E-09 -1.06E-09 -8.78E-10 -6.92E-140.43E-109.48E-11 -5.27E-10 -1.40E-09   2.90E-095.15E-091.17E-08
$
 -1.42E-09 -1.23E-09 -1.02E-09 -8.13E-150.38E-101.66E-10 -4.55E-10 -1.27E-09   2.53E-094.18E-097.11E-09
1.45E-08
$
 -1.53E-09 -1.36E-09 -1.17E-09 -9.80E-170.35E-104.09E-10 -1.12E-10 -7.43E-10   1.63E-092.66E-094.02E-09
5.68E-091.45E-08
$
 -1.34E-09 -1.20E-09 -1.03E-09 -8.75E-160.67E-103.88E-10 -5.49E-11 -5.78E-10   1.29E-092.08E-093.03E-09
4.02E-097.10E-091.17E-08
$
 -1.12E-09 -1.01E-09 -8.69E-10 -7.47E-150.82E-103.57E-101.33E-12 -4.09E-10      9.46E-101.49E-092.08E-09
2.66E-094.17E-095.15E-098.96E-09
$
 -9.12E-10 -8.28E-10 -7.26E-10 -6.41E-150.19E-103.48E-106.80E-11 -2.42E-10      6.15E-109.47E-101.29E-09
1.63E-092.53E-092.90E-093.68E-096.95E-09
$
 -6.26E-10 -5.84E-10 -5.24E-10 -4.85E-140.19E-103.17E-101.44E-10 -4.11E-11      2.42E-104.09E-105.78E-10
7.43E-101.27E-091.41E-091.61E-092.04E-094.66E-09
$
 -2.79E-10 -2.86E-10 -2.77E-10 -2.89E-120.89E-102.69E-102.12E-101.43E-10 -6.77E-11 -9.87E-13   5.51E-11
1.12E-104.55E-105.26E-106.17E-107.90E-101.18E-093.41E-09
$
        3.51E-102.67E-101.96E-10  1.14E-10 -1.67E-11  8.69E-11  1.85E-10  2.40E-10 -2.79E-10 -2.99E-10 -
3.37E-10 -3.65E-10 -2.13E-10 -1.52E-10 -7.38E-11  3.51E-11  2.29E-10  6.49E-10  3.27E-09
$
  1.03E-09  8.07E-10  6.08E-10  4.02E-10 -1.63E-10  7.27E-11  2.89E-10  4.19E-10 -5.20E-10 -5.82E-10 -6.67E-
10 -7.35E-10 -5.37E-10 -4.43E-10 -3.23E-10 -1.81E-10  4.01E-11  4.07E-10  1.16E-09  5.31E-09
$
  1.98E-09  1.58E-09  1.20E-09  8.14E-10 -4.01E-10 -3.21E-11  2.89E-10  4.85E-10 -6.41E-10 -7.47E-10 -8.75E-
10 -9.80E-10 -8.12E-10 -6.92E-10 -5.42E-10 -3.80E-10 -1.39E-10  2.17E-10  8.58E-10  2.55E-09  7.44E-09
$
```

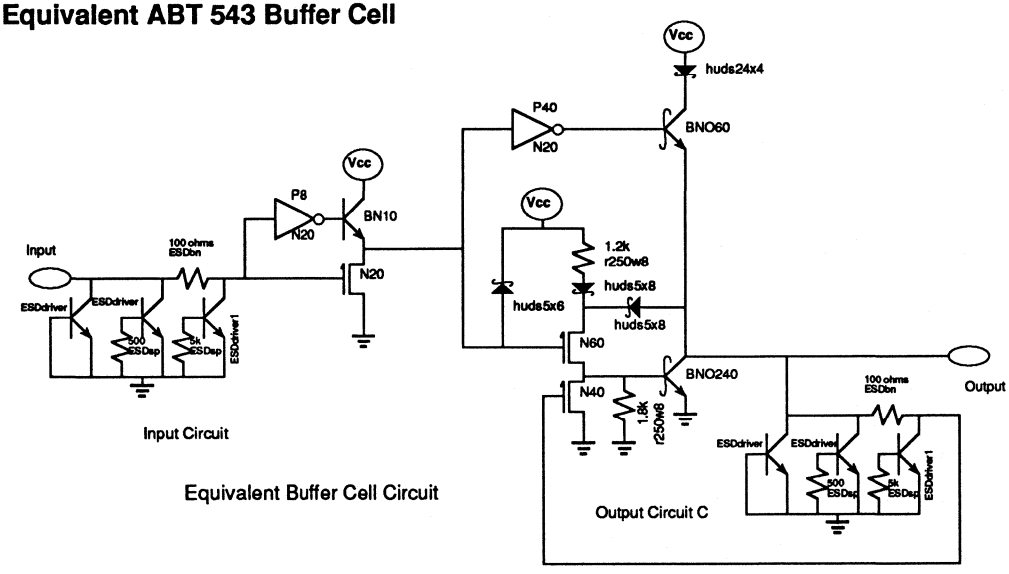
```
  3.12E-09  2.45E-09  1.81E-09  1.20E-09 -6.08E-10 -1.25E-10  2.77E-10  5.23E-10 -7.26E-10 -8.69E-10 -1.03E-
09 -1.17E-09 -1.02E-09 -8.78E-10 -7.02E-10 -5.19E-10 -2.58E-10  1.01E-10  7.20E-10  2.01E-09  4.20E-09
9.58E-09
$
  4.59E-09  3.47E-09  2.45E-09  1.58E-09 -8.07E-10 -2.04E-10  2.86E-10  5.84E-10 -8.28E-10 -1.00E-09 -1.20E-
09 -1.36E-09 -1.23E-09 -1.06E-09 -8.52E-10 -6.43E-10 -3.55E-10  2.25E-11  6.46E-10  1.74E-09  3.33E-09
5.79E-09  1.22E-08
$
  6.48E-09  4.59E-09  3.12E-09  1.98E-09 -1.03E-09 -3.01E-10  2.79E-10  6.26E-10 -9.11E-10 -1.12E-09 -1.34E-
09 -1.53E-09 -1.42E-09 -1.22E-09 -9.87E-10 -7.56E-10 -4.44E-10 -5.01E-11  5.82E-10  1.56E-09  2.89E-09
4.67E-09  7.69E-09  1.51E-08
$
$
$ Coupling Coefficients k
$  1.00E+00
$  5.67E-01  1.00E+00
$  3.89E-01  5.38E-01  1.00E+00
$  2.73E-01  3.50E-01  4.99E-01  1.00E+00
$ -1.75E-01 -2.17E-01 -2.82E-01 -4.07E-01  1.00E+00
$ -8.51E-02 -1.08E-01 -1.39E-01 -1.93E-01  3.17E-01  1.00E+00
$  6.95E-03 -3.46E-03 -1.76E-02 -4.30E-02  9.54E-02  2.30E-01  1.00E+00
$  5.29E-02  4.71E-02  3.87E-02  2.36E-02  8.03E-03  8.38E-02  2.96E-01  1.00E+00
$ -7.39E-02 -6.99E-02 -6.37E-02 -5.29E-02  2.99E-02 -2.48E-02 -1.62E-01 -3.58E-01  1.00E+00
$ -8.49E-02 -8.15E-02 -7.59E-02 -6.64E-02  4.68E-02  5.52E-04 -1.12E-01 -2.51E-01  4.67E-01  1.00E+00
$ -9.20E-02 -8.88E-02 -8.33E-02 -7.43E-02  5.63E-02  1.44E-02 -8.35E-02 -1.90E-01  3.23E-01  5.04E-01
1.00E+00
$ -9.58E-02 -9.25E-02 -8.69E-02 -7.83E-02  6.13E-02  2.26E-02 -6.47E-02 -1.54E-01  2.52E-01  3.66E-01  5.47E-
01  1.00E+00
$ -1.04E-01 -1.02E-01 -9.91E-02 -9.43E-02  8.38E-02  5.56E-02 -1.59E-02 -9.04E-02  1.63E-01  2.33E-01  3.09E-
01  3.92E-01  1.00E+00
$ -1.01E-01 -1.01E-01 -9.77E-02 -9.40E-02  8.48E-02  5.88E-02 -8.71E-03 -7.84E-02  1.44E-01  2.03E-01  2.60E-
01  3.09E-01  5.46E-01  1.00E+00
$ -9.64E-02 -9.62E-02 -9.40E-02 -9.16E-02  8.44E-02  6.18E-02  2.40E-04 -6.33E-02  1.20E-01  1.66E-01  2.03E-
01  2.33E-01  3.66E-01  5.04E-01  1.00E+00
$ -8.91E-02 -9.00E-02 -8.91E-02 -8.92E-02  8.55E-02  6.83E-02  1.40E-02 -4.26E-02  8.84E-02  1.20E-01  1.44E-
01  1.63E-01  2.52E-01  3.23E-01  4.67E-01  1.00E+00
$ -7.47E-02 -7.75E-02 -7.86E-02 -8.23E-02  8.43E-02  7.62E-02  3.60E-02 -8.83E-03  4.26E-02  6.34E-02  7.84E-
02  9.04E-02  1.54E-01  1.91E-01  2.50E-01  3.58E-01  1.00E+00
$ -3.88E-02 -4.43E-02 -4.86E-02 -5.74E-02  6.79E-02  7.55E-02  6.21E-02  3.59E-02 -1.39E-02 -1.79E-04  8.73E-
03  1.60E-02  6.46E-02  8.34E-02  1.12E-01  1.62E-01  2.96E-01  1.00E+00
$  5.00E-02  4.23E-02  3.51E-02  2.32E-02 -4.01E-03  2.49E-02  5.53E-02  6.16E-02 -5.86E-02 -5.54E-02 -5.46E-
02 -5.31E-02 -3.09E-02 -2.47E-02 -1.36E-02  7.36E-03  5.88E-02  1.94E-01  1.00E+00
$  1.15E-01  1.00E-01  8.54E-02  6.39E-02 -3.07E-02  1.63E-02  6.80E-02  8.44E-02 -8.56E-02 -8.44E-02 -8.48E-
02 -8.38E-02 -6.13E-02 -5.63E-02 -4.69E-02 -2.99E-02  8.06E-03  9.57E-02  2.78E-01  1.00E+00
$  1.87E-01  1.66E-01  1.42E-01  1.09E-01 -6.39E-02 -6.09E-03  5.74E-02  8.23E-02 -8.92E-02 -9.16E-02 -9.40E-
02 -9.44E-02 -7.82E-02 -7.43E-02 -6.64E-02 -5.29E-02 -2.37E-02  4.31E-02  1.74E-01  4.07E-01  1.00E+00
$  2.60E-01  2.27E-01  1.89E-01  1.42E-01 -8.52E-02 -2.09E-02  4.85E-02  7.84E-02 -8.90E-02 -9.38E-02 -9.75E-
02 -9.89E-02 -8.67E-02 -8.31E-02 -7.58E-02 -6.36E-02 -3.86E-02  1.77E-02  1.29E-01  2.81E-01  4.98E-01
1.00E+00
$  3.38E-01  2.84E-01  2.27E-01  1.66E-01 -1.00E-01 -3.02E-02  4.43E-02  7.73E-02 -8.99E-02 -9.60E-02 -1.00E-
01 -1.02E-01 -9.23E-02 -8.86E-02 -8.14E-02 -6.98E-02 -4.70E-02  3.49E-03  1.02E-01  2.17E-01  3.49E-01
5.35E-01  1.00E+00
$  4.29E-01  3.38E-01  2.60E-01  1.87E-01 -1.15E-01 -4.00E-02  3.88E-02  7.46E-02 -8.89E-02 -9.62E-02 -1.01E-
01 -1.04E-01 -9.57E-02 -9.19E-02 -8.48E-02 -7.38E-02 -5.29E-02 -6.97E-03  8.28E-02  1.74E-01  2.73E-01
3.88E-01  5.66E-01  1.00E+00
```

D. An example of PSPICE netfile.

```
*Ref simulations*
.TRAN .1ns 30ns
.LIB \MODELS\QBMODELS.LST
.PROBE
.WIDTH OUT=80
.OPTIONS ITL5=25000 ACCT NOMOD
.SUBCKT abt543d 1 2 50 60
```

```
* Pin 1 is Input
* Pin 2 in Output Pin
* Pin 50 is Vcc
* Pin 60 is Gnd
R1 4 60 500
R2 5 60 5k
R3 6 1 100
R4 50 12 1.2k
R5 15 60 1.2k
R6 16 60 500
R7 17 60 5k
R8 2 18 100
Q1 1 60 60 60 ESDdriver
Q2 1 4 60 60 ESDdriver
Q3 6 5 60 60 ESDdriver1
Q4 50 7 8 60 BN10
XQ6 10 9 2 60 BNO60
XQ7 2 15 60 60 BNO240
Q8 2 60 60 60 ESDdriver
Q9 2 16 60 60 ESDdriver
Q10 18 17 60 60 ESDdriver
XD1 50 10 60 huds24x4
XD2 8 50 60 huds5x6
XD3 12 13 60 huds5x8
XD4 2 13 60 huds5x8
M1 50 6 7 50 MHS4PEN L=1.2E-6 W=7.298E-6 AD=14.6p AS=14.6p PD=18.6u
+ PS=18.6u NRD=.274 NRS=.274
M2 7 6 60 60 MHS4NEN L=1.2E-6 W=19.926E-6 AD=39.85p AS=39.85p PD=43.8u
+ PS=43.8u NRD=.1 NRS=.1
M3 50 8 9 50 MHS4PEN L=1.2E-6 W=39.298E-6 AD=79.85p AS=79.85p PD=83.85u
+ PS=83.85u NRD=.05 NRS=.05
M4 9 8 60 60 MHS4NEN L=1.2E-6 W=19.926E-6 AD=39.85p AS=39.85p PD=43.8u
+ PS=43.8u NRD=.1 NRS=.1
M7 8 6 60 60 MHS4NEN L=1.2E-6 W=19.928E-6 AD=39.85p AS=39.85p PD=43.8u
+ PS=43.8u NRD=.1 NRS=.1
M9 13 8 15 60 MHS4NEN L=1.2E-6 W=59.926E-6 AD=120p AS=120p PD=124u
+ PS=124u NRD=.0333 NRS=.0333
M10 15 18 60 60 MHS4NEN L=1.2E-6 W=39.926E-6 AD=79.85p AS=79.85p PD=83.85u
+ PS=83.85u NRD=.05 NRS=.05
.ENDS
VCC 5 0 DC 5
Vin 1 0 PULSE 3 0 5ns 2.5ns 2.5ns 10ns 100ns
C1 2 0 50pF
R1 2 0 500
L1 1 11 2.5nH
L2 2 12 2.5nH
L3 5 15 10nH
L4 10 0 10nH
Xdri 11 12 15 10 abt543d
.END
```

Equivalent ABT 543 Buffer Cell



Input Circuit

Equivalent Buffer Cell Circuit

Output Circuit C

Printed circuit board test fixtures for high-speed logic

AN602

INTRODUCTION

The Signetics Standard Products Group (SPG) operates a Characterization Laboratory in Orem, Utah. This Lab maintains the capability of testing the 11 logic product families the Division supports. These include: AuTTL–74XXX, Schottky-74SXXX, Low-Power Schottky-74LSXXX, FAST–74FXXX, ALS-74ALSXXX, High-Speed CMOS-74HCXXX, High-Speed CMOS/TTL-74HCTXXX, Advanced CMOS/TTL (ACL)-74ACT11XXX, Advanced CMOS (ACL)-74AC11XXX, Advanced BiCMOS (ABT)-74ABTXXX, and both 10K and 100K ECL.

In the past Signetics SPG Characterization has designed and built a series of bench test AC fixtures that provide the ability to have one fixture that addresses many product types across families. It allowed the use of a smaller fixture inventory to perform well over the majority of the devices. With the advent of the 74ACL11xxx and 74ABTXXX series the existing fixtures were no longer adequate. The largest problem with the older fixtures is the method of bypassing switching noise from V_{CC} to GND. They use bus bars running down the top and bottom sides of the PC board from the end of the device to the point of connection to the DUT V_{CC}/GND pins. Connection was then made using a copper braid to the DUT pin. While adequate for earlier logic families there is too much inductance in the power supply path to allow switching the faster transitions and higher currents of the ACL and ABT families without causing severe aberrations in output waveforms. These families of devices are also the first "TTL" types to specify operation over the entire V_{CC}/GND extremes in a simultaneous switching condition.

THEORY OF OPERATION

There are several key points in testing the ABT and ACL families. They are:

- Low inductance/high frequency power supply by-passing.
- Large ground and V_{CC} planes (covering virtually the entire board area).
- 50Ω signal lines for uniform impedance, high bandwidth and easy interface to test gear.

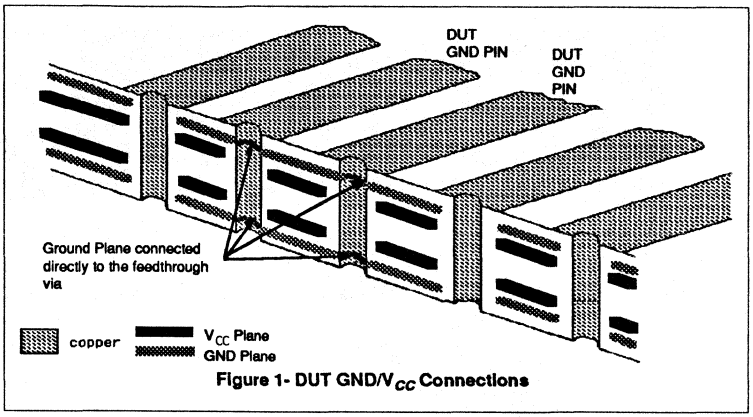


Figure 1- DUT GND/V_{CC} Connections

- Output AC load capacitance close to the DUT.
- Measurement point close to the DUT.

POWER SUPPLY AND GROUND

The largest difference between these fixtures and the earlier series is the inclusion of dedicated GND and other power supply planes internal to the PC board. The GND layers are used for impedance control of the signal traces and internal to the GND planes are V_{CC} and other power supply planes. In order to provide the lowest possible impedance in the power and GND connections the planes are connected directly to the DUT power/GND pad vias (See Figure #1). This feature reduces the V_{CC}/GND path inductances to a minimum and provides the highest possible frequency response under simultaneous switching conditions. This series of boards has a ring frequency of approximately 500 MHz between the power supply pins. This ensures that the output waveforms seen on the test equipment are due to the device and package, not the fixture. The trade-off for these features is that the boards must be purchased for a particular V_{CC}/GND pin combination. Signetics has designated an extension to the DUT board PC board numbers to allow calling out the separate internal layers needed for the various GND/power supply combinations. See Appendix I for the GND/V_{CC} combinations.

DEVICE SOCKETS

These boards do not use a DUT socket. All surface mount packages in this series of PC boards use a conductive polymer from Shin-Etsu for signal transmission (See Figure #3). This polymer, type MAF, only conducts in the vertical direction and provides a low impedance path to connect between the DUT leads and the PC board pad. DIP pattern boards use Augat sockets soldered flush with the PC board surface. This effectively eliminates any inductance due to a socket. The trade-off is decreased insertions on the surface mount boards. In order to align an SMT device to the required DUT pads alignment blocks and alignment guides are required (See Appendix I for dimensions). They are machined from a phenolic material for over temperature operation and electrical isolation. The block is designed to align the DUT to the pads, allow circulation for a temperature stream and on gull-wing devices, to provide mechanical pressure to the leads to ensure contact with the conductive polymer. The top hole in the block also doubles as the vacuum wand access to change devices. The boards are also designed to use the alignment guides to provide a mechanical clamp and hold the polymer in place and allow easy replacement. See Figure #4.

SIGNAL LINES

All signal lines have a 50Ω impedance, determined by the microstrip layout method. The 50Ω value was selected to allow easy termination for input signal generators and a 10:1 divider for out-

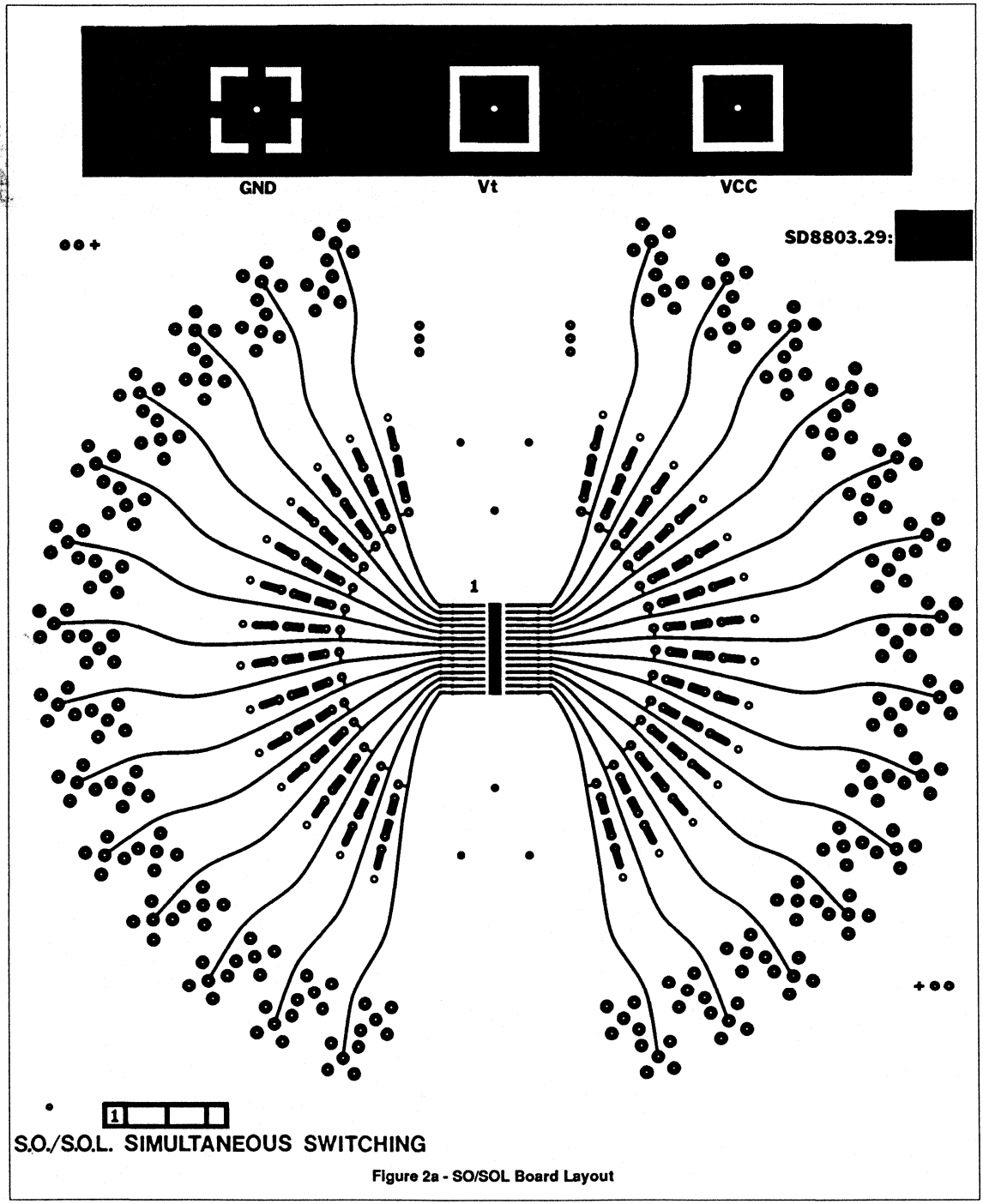


Figure 2a - SO/SOL Board Layout

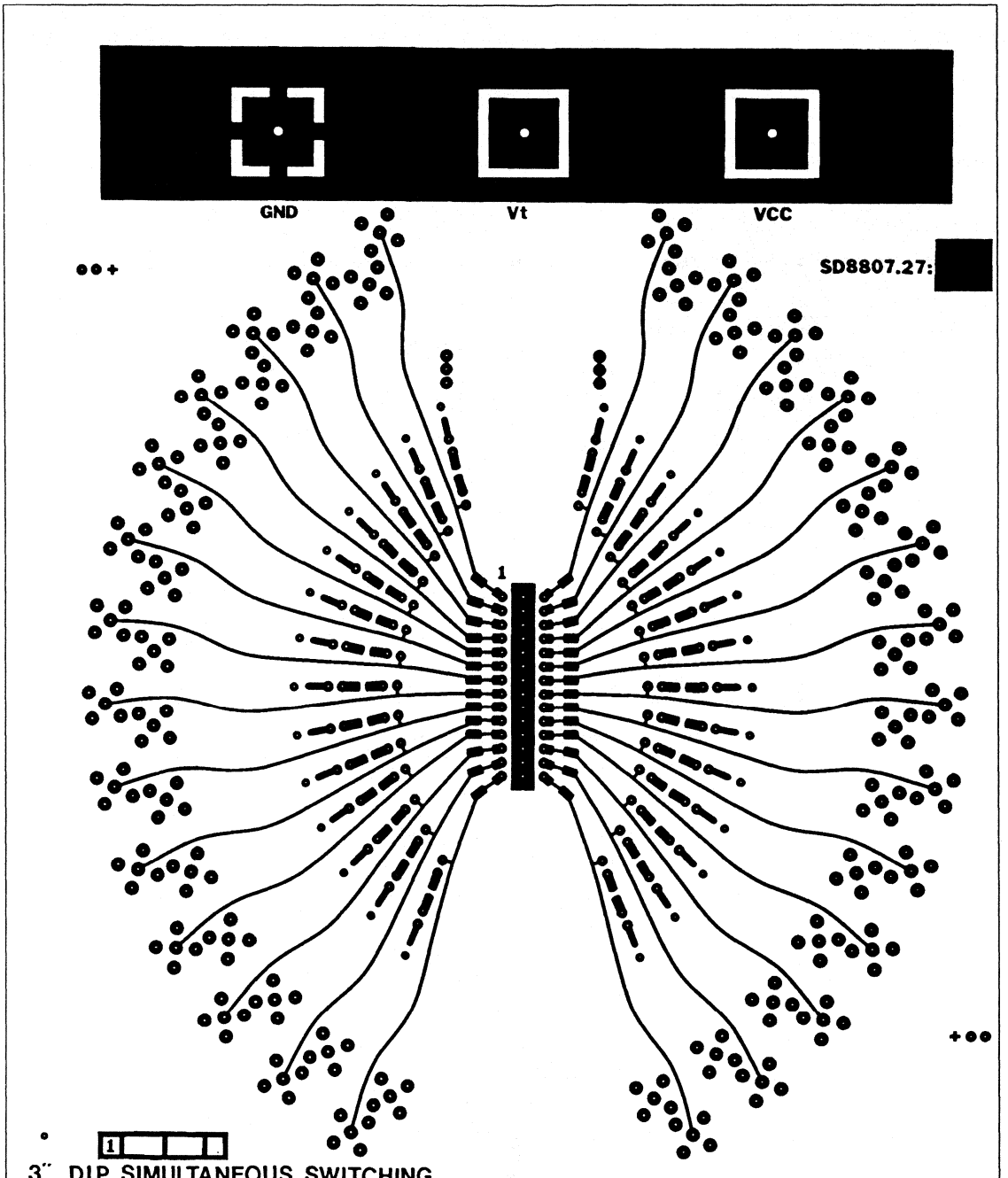


Figure 2b - .3" DIP Board Layout

puts. The inputs are also terminated into a 10:1 divider, 50Ω terminator. This allows the boards to be built with very small stubs for signal integrity and all oscilloscope channels can be set up to the same vertical amplification.
On the top of the PC board is a trace running straight from the SMB connector to the DUT pad. The only connection to this line is a jumper allowing connection of a pull-up resistor for TTL 3-S or open-collector outputs. On the bottom of the PC board the trace has a break in it to allow mounting a 453Ω resistor (R1) for the 10:1 divider network. Since the worst case load in simultaneous switching conditions is to mount a lumped capacitance directly on the DUT pin, a direct connection to the internal GND plane is in the center of the DUT pads to allow soldering on load capacitors. For input pins it is also used for mounting termination resistors directly beneath the device. Therefor the

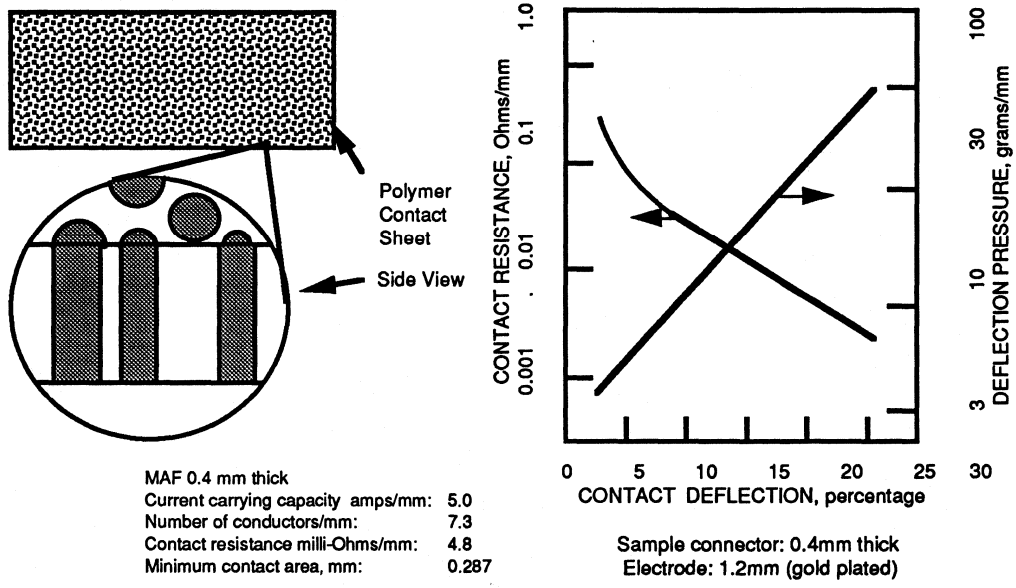


Figure 3 - Shin-Etsu Polymer

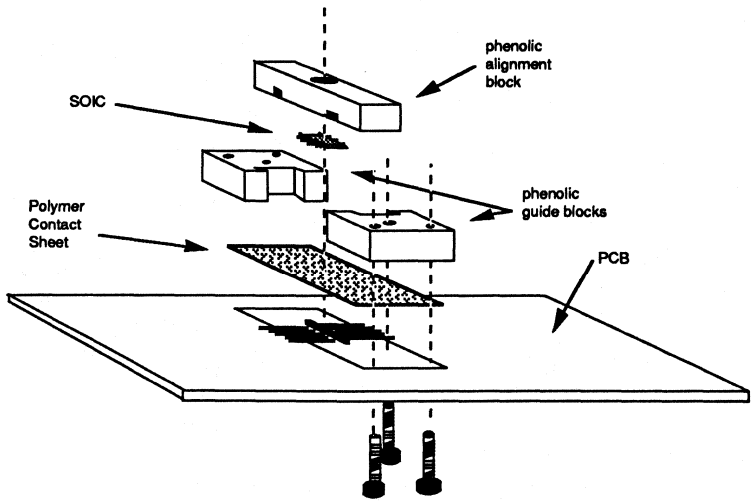


Figure #4. Illustrated Parts Breakout of SO Device Assembly

Printed circuit board test fixtures for high-speed logic AN602

PC boards must be assembled for a particular I/O pin combination.

If a DUT pin is an input the board is configured in a loop through mode. The outer circle of SMB connectors is connected to the signal source. On the bottom side of the PC board a 56.2Ω (R2) resistor is soldered between the DUT pad and the GND. Across the break in the bottom trace a 453Ω resistor is soldered. In combination with a 50Ω o-scope termination or a 50Ω SMB terminator the 450 + 50Ω in parallel with the 56.2Ω provides the proper 50Ω termination for signals and a monitoring capability (See Figure 5a).

For an output pin the outer ring of SMB's is not used. The same 453Ω/50Ω pair is used as a 10:1 divider into

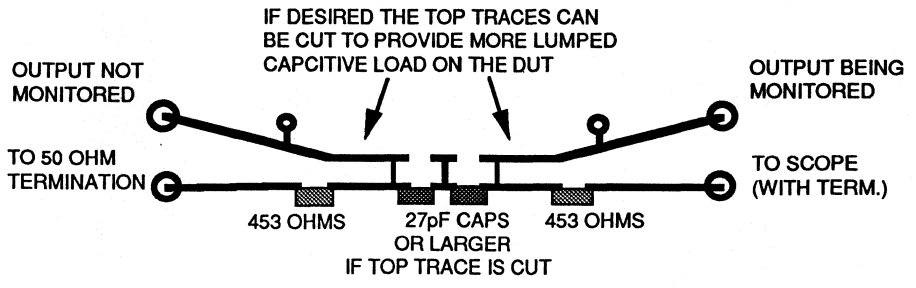


Figure 5a - SSE PC Board Input Schematics

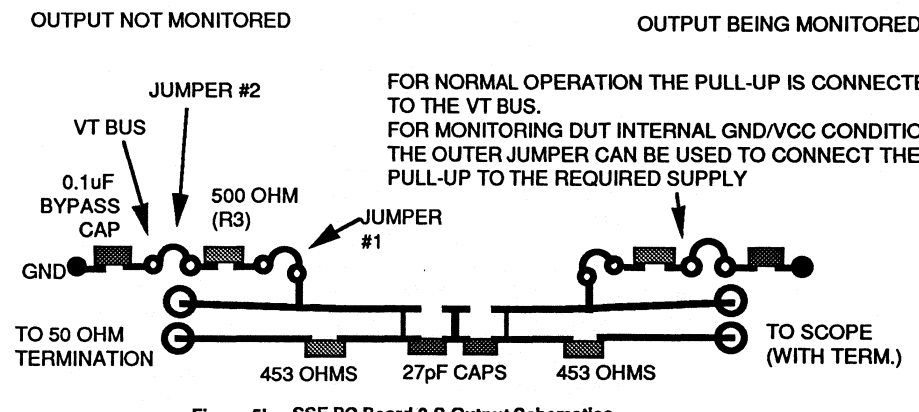


Figure 5b - SSE PC Board 2-S Output Schematics

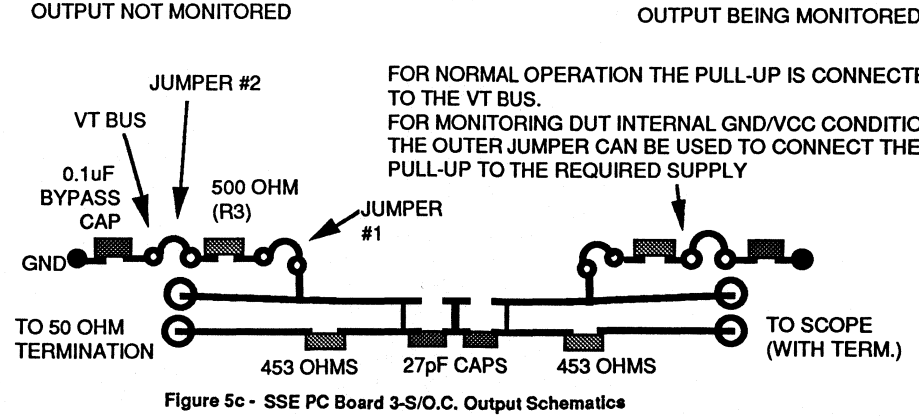


Figure 5c - SSE PC Board 3-S/O.C. Output Schematics

the o-scope and still provide the specified 500Ω pull-down resistor. A chip capacitor of sufficient capacitance to bring the total to 50pF is soldered between the bottom DUT pad and the GND (See Figure 5b). For 3-S or open collector devices the 500Ω pull-up resistor (R3) on the top trace is jumpered in with a .1" jumper (#1). The outside of the pull-up resistor also has a .1" jumper (#2) to allow connection to the internal V_T bus or some other termination voltage as needed for any particular test (See Figure 5c).

The bottom trace SMB connector is always connected either to an SMB 50Ω terminator or the 50Ω terminated input of the scope to complete the load. See Figure 6 for a 50Ω terminator example.

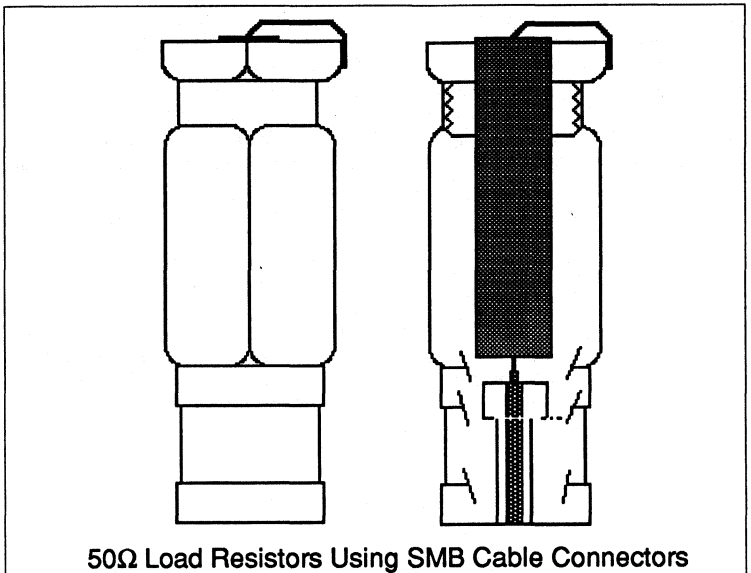


Figure 6 - Resistive Load Used on Non-monitored SMB Connectors

INPUT STIMULUS AND MEASUREMENT

As stated previously, the measurements are made with 50Ω sampling systems. The connections to these systems are made via SMB connectors. This was chosen since it is a standard connector, available from several sources, uses push-on operation, is small for easy configuration and is capable of high bandwidth operation. Figure 8 shows where the connections are made and also where the pulse generators connect to the input, also an SMB connector. Since the 450Ω resistor, R1, is soldered directly to the pin of the device, see Figure 6, the actual probe tip is at that point. This has the advantage of eliminating any distance from the device to the probe tip, thus guaranteeing accurate results.

INSERTING DEVICES

To hold surface mount devices in place the alignment block is clipped down to the PC board with brass clips mounted to the alignment guides. This provided the simplest solution to several conflicting demands. The device had to have good contact with the Shin-Etsu polymer to function. There needed to be some method of allowing a temperature stream flow around the device, and the devices needed to be changed. For SO devices the edges of the package cutout provide enough pressure to the top of the DUT leads to make good contact with the polymer, for PLCC the top of the cutout provides the same function. The hole through the middle of the alignment block allows a vacuum wand to be inserted and hold the device and block together until they are clipped to the PC board. Several models of wands are available from H-Square Company for handling devices, including one with a built in static dissipation resistor and lead for ESD protection. They also have designed a custom tip to mate with the top hole of the alignment blocks and prevent the block from bouncing up the wand tube prior to clipping it to the PC board. Cutouts around the device allow exit for the temperature stream.

VERSATILITY AND COST

At some point, there is a choice between the most technically attractive options and the cost of such options. This fixture has been designed to optimize its technical effectiveness. This was dictated by the test requirements of the ACL and ABT families, specifically the simultaneous switch specifications. It is also suitable for testing FAST, ALS and ECL product devices if the existing series of boards do not provide the needed environment to get accurate, repeatable results.

For the user the only connections being made to the fixture are:

- V_{CC} (banana jack) This is the positive DUT voltage supply.
- GND (banana jack) This is the common ground of all input supplies.
- V_T supply (banana jack) This is the 3-state/O.C. pull-up voltage and is jumpered to each pin as needed.
- V_{GND} supply (banana jack) This is the DUT GND layer used for ECL which requires a +2V offset for proper termination on the output pins when using oscilloscope input termination.
- V_{EE} supply (banana jack) This is the negative DUT power supply layer used for ECL devices
- Input Stimulus (outside SMB connectors) This is found on every input/output pin. More than one pin may be used in this manner.
- Output Measurement or Scope Connection (inside SMB connectors). More than one pin may be used in this manner. *Remember*, if this pin

is not connected to a scope, a 50Ω resistor must be connected here to ground to complete the 500Ω resistive load or input termination network. Signetics has constructed their own 50Ω load by soldering a high quality (high frequency) 50Ω resistor inside a female SMB cable connector. See Figure 6.

With these seven connection types, the fixture is capable of testing the product lines mentioned.

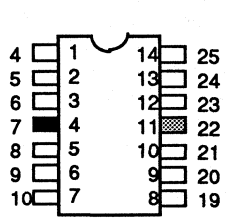
Included in Appendix I are the internal GND/V_{CC} connections of the existing defined layers.

In Appendix II are the dimensions of the alignment blocks and guides for the SMT packages.

In Appendix III is the parts list for these fixtures and the supplies used by Signetics.

This in no way constitutes Signetics endorsements of these suppliers and the customer may select their own supplier if they so desire. This fixture is offered to the public to duplicate and use within their own environments. Signetics will not provide any materials but will allow the manufacturers of the board and materials to build and/or supply for any requesting party. Pricing and availability are left to the vendors and Signetics has no control over those issues. The intent is to provide something for users of ACL and ABT, and other advanced logic family devices, that has been proven and tested in use, namely the characterization of these products prior to the introduction to the market place.

Appendix I - Internal GND/V_{CC} Connections



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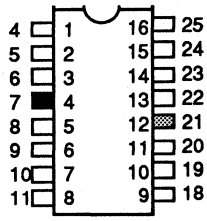

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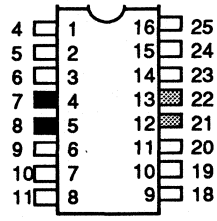

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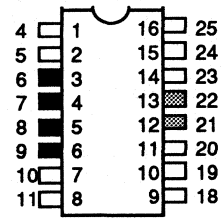

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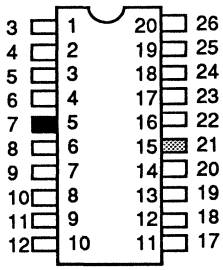

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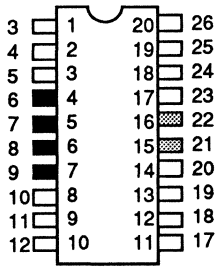

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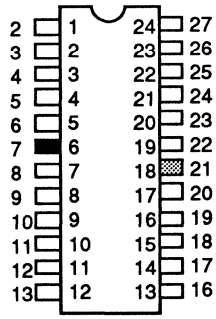

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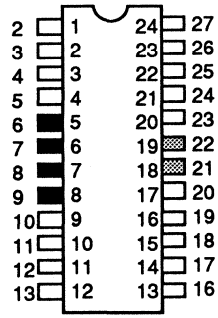
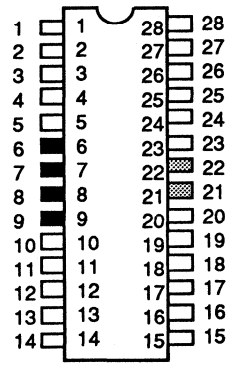


SD8803.29:004

VCC ▩
GND ■

(On each package outline the outer numbers refer to the PCB footprint and the inner numbers refer to the DUT pins.)

For .3" DIP boards, substitute SD8807.27:nnn for SD8803.29:nnn



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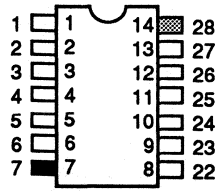
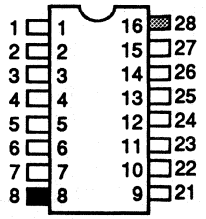


SD8803.29:005



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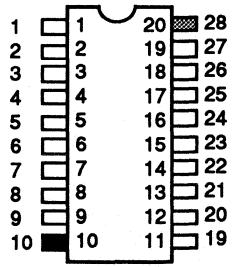

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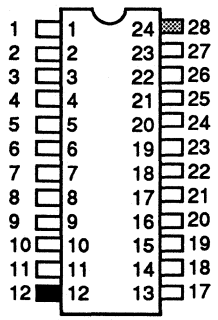
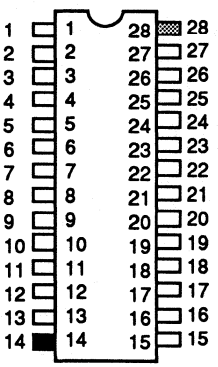


SD8803.29:008



SD8803.29:009

VCC GND

NOTE: The PC board/package configurations shown above require the use of the SO alignment blocks with offset package cutouts.

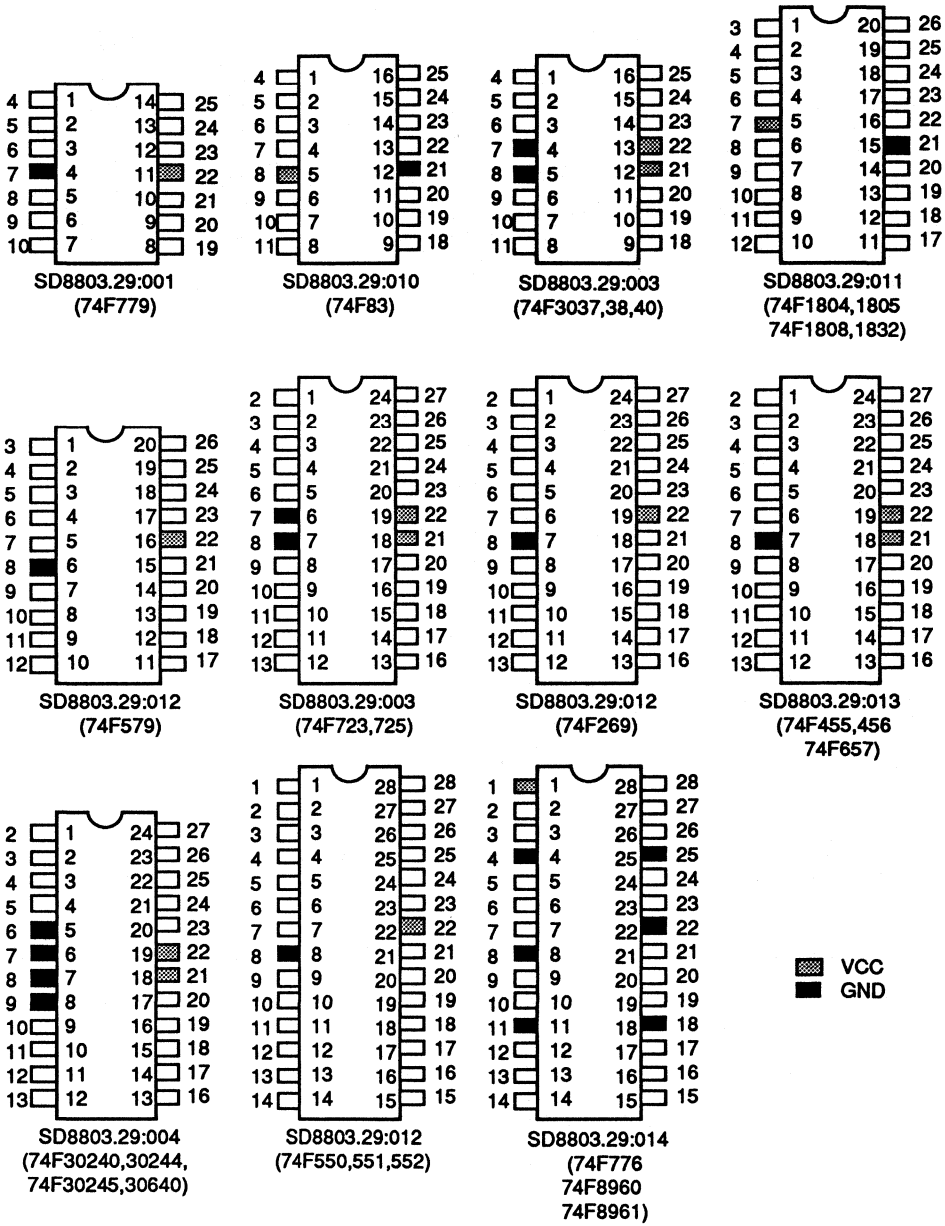
Defined layers and their connections for SO (SD8803.29:nnn) and .3" DIP (SD8807.27:nnn) boards are:

GROUND LAYER (2.x)	
2.1 =	7
2.2 =	7, 8
2.3 =	10
2.4 =	6, 7, 8, 9
2.5 =	21, 22
2.6 =	21
2.7 =	8
2.8 =	12
2.9 =	14
2.A =	4, 8, 11, 18, 22, 25

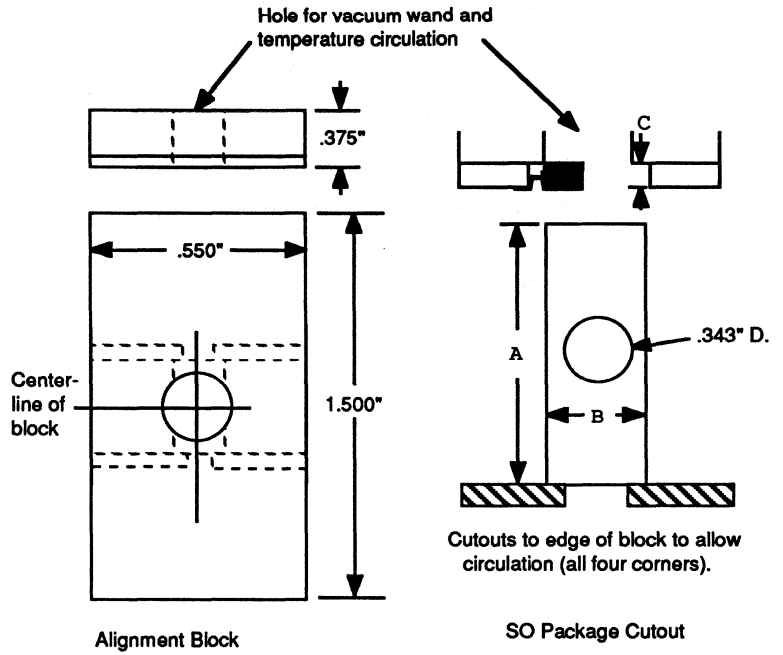
V_{CC} LAYER (3.y)	
3.1 =	22
3.2 =	21, 22
3.3 =	28
3.4 =	21
3.5 =	8
3.6 =	7
3.7 =	1

Printed circuit board test fixtures for high-speed logic

AN602



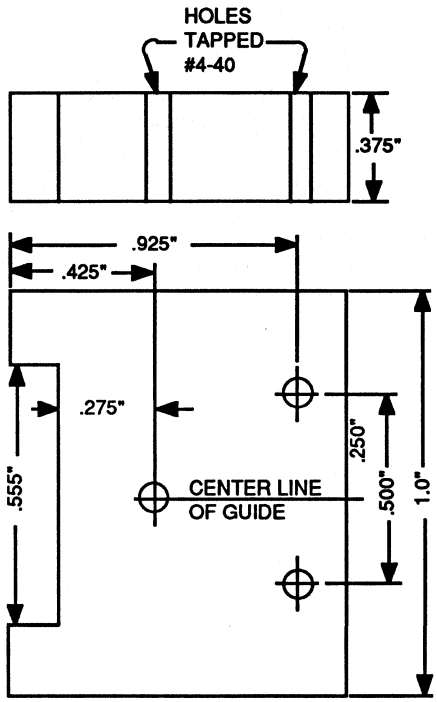
APPENDIX II - SMT Alignment Blocks and Guides



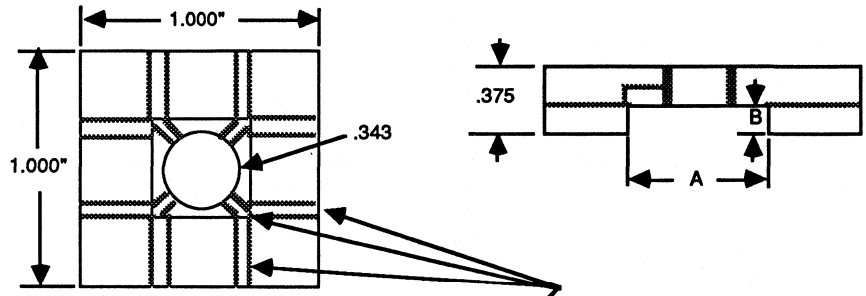
Material phenolic or other insulator able to withstand 155°C.

DIMENSIONS FOR VARIOUS SIGNETICS PRODUCED PACKAGES

PACKAGE		A	B	C	OFFSET FROM CENTERLINE
JEDEC	14 PIN .150"	.346 +-.001	.205	.055+-.001	.025
JEDEC	14 PIN .150"	.346 +-.001	.205	.055+-.001	.175
EIAJ II	14 PIN .210"	.405 +-.001	.265	.075+-.001	.025
EIAJ II	14 PIN .210"	.405 +-.001	.265	.075+-.001	.175
JEDEC	16 PIN .150"	.400 +-.001	.200	.050+-.001	.000
JEDEC	16 PIN .150"	.400 +-.001	.200	.050+-.001	.150
EIAJ II	16 PIN .210"	.405 +-.001	.265	.070+-.001	.000
EIAJ II	16 PIN .210"	.405 +-.001	.265	.070+-.001	.150
JEDEC	16 PIN .300"	.406 +-.001	.360	.090+-.003	.000
JEDEC	16 PIN .300"	.406 +-.001	.360	.090+-.003	.150
EIAJ II	20 PIN .210"	.505 +-.001	.265	.075+-.001	.000
EIAJ II	20 PIN .210"	.505 +-.001	.265	.075+-.001	.100
JEDEC	20 PIN .300"	.510 +-.001	.365	.095+-.003	.000
JEDEC	20 PIN .300"	.510 +-.001	.365	.095+-.003	.100
JEDEC	24 PIN .300"	.605 +-.001	.365	.095+-.003	.000
JEDEC	24 PIN .300"	.605 +-.001	.365	.095+-.003	.050
JEDEC	28 PIN .300"	.710 +-.001	.365	.090+-.003	.000



SO Alignment Guides

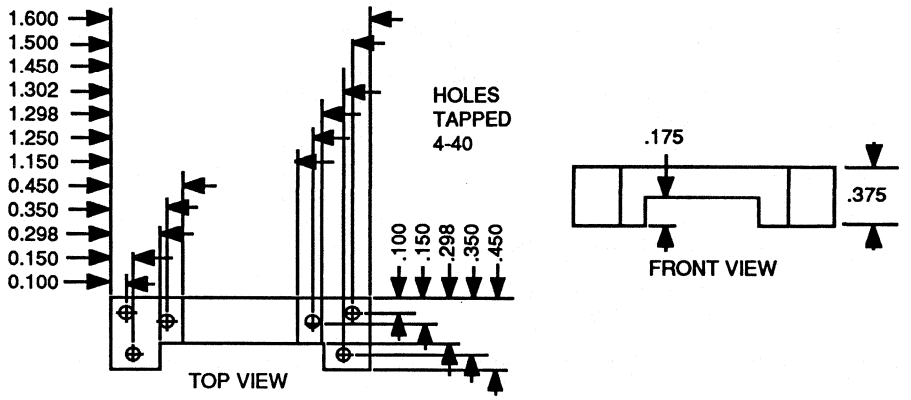


Cutouts from center hole to edge of block to allow circulation around device when forcing temperature (all four corners).

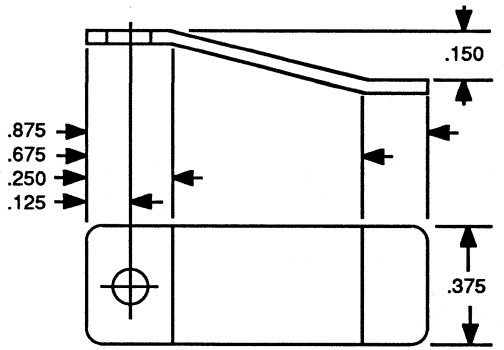
PACKAGE TYPE	A	B
20 PIN PLCC	.390"	.160"
20 PIN LCC	.350"	.060"
28 PIN PLCC	.494"	.160"
28 PIN LCC	.450"	.060"

Figure 12 - PLCC/LCC Alignment Block and Package Cutout Dimensions

Printed circuit board test fixtures for high-speed logic AN602



PLCC/LCC Alignment Guide



Hole .116 +- .003" diameter.
.020" Brass shim stock
Edges deburred
Corners radiused .050"

All other dimensions +- .025"

Alignment Block Retainer Clip

APPENDIX III - Component and Vendor List and Construction Hints

The following prices have been quoted for a 10 piece build of a 28 pin test fixture and are not binding in any way.

1. Printed circuit board, requirement: 1 per part configuration.

BOARD	PART #	COST	
SO and SOL	SD8803.29:nnn	$160.00	
DIP	SD8807.27:nnn	$160.00	
PLCC (20/28 pin)	SD8901.20:nnn	$160.00	(6 layer)
PLCC (20/28 pin)	SD8901.20:nnn	$182.65	(8 layer)

Supplier: Prototype and Production Circuits
8040 S. 1444 W.
West Jordan, UT 84084
(801) 566-5431

2. Conductive Polymer Shin-Etsu# to Available in sheets of 0.2 to 0.8 mm in thickness in 0.1 mm steps and 50 mm X 100 mm.

(0.2 mm)	MAF2tx50x100	$70.00 @	
(0.4 mm)	MAF4tx50x100	$77.00 @	(recommended)
(0.6 mm)	MAF6tx50x100	$81.00 @	

Supplier: Shin-Etsu Polymer,
SP America Inc.
34135 7th Street
Union City, CA 94587
(415) 475-9000

3. Ceramic multilayer chip capacitors from Johanson Dialectrics.

27 pF	101R09N270JP (5%)	$0.45 @ in 1000's
33 pF	101R09N330JP (5%)	$0.45 @ in 1000's

Supplier: Johanson Dialectrics
2220 Screenland Drive
Burbank, CA 91505
(213) 848-4465

4. Tantalum dipped capacitors from Sprague.

4.7 uF, 35 V	196D475X9035JA1	$0.63 @ 50's

Supplier: Newark Electronics

5. Ceramic chip resistors from Dale Electronics, Inc or Bourns, Inc.

453 Ohm (Dale)	CRCW0805-4530F (1%)	$137.00/Reel (1000 or 5000)
56.2 Ohm	CRCW0805-56R2F (1%)	(These are also available in a
500 Ohm	CRCW0805-4990F (1%)	CRCW1206 size.)
453 Ohm (Bourns)	CR0805-4530FVBA (1%)	$100.00/Reel (5000)
56.2 Ohm	CR0805-56R2JVBA (5%)	(These are also available in a
500 Ohm	CR0805-4990FVBA (1%)	CR1206 size.)

Suppliers: Dale Electronics, Inc.
2300 Riverside Blvd.
Norfolk, NE 68701
(402) 371-0080

Bourns, Inc
1200 Columbia Avenue
Riverside, CA 92507
(714)781-5500

6. SMB connectors from Applied Engineering Products.

SMB Straight Male Jack Receptacle		
	2009-1511-000	$2.19 @ in 100-250's
SMB Straight Female Cable Plug for RG-174 coax		
	2002-1551-003	$3.59 @ in 100-250's
SMB Tee Adaptor (Jack-Plug-Jack)		
	5215-1501-000	$12.51 @ in 50-99's
SMB Tee Adaptor (Plug-Plug-Jack)		
	5235-1501-000	$17.26 @ in 1-24's

Supplier: Spirit Electronics, Inc
7819 East Greenway, Suite 9
Scottsdale, AZ 85206
(602) 998-1533

7. Sockets-pins and jumpers from Augat.

Socket Terminal Pin	LSG-1AG14-14	$0.20 @ in 1000's
Jumpers (.1")	8156-651P2	$0.05 @ in 1000's

Supplier: Augat, Inc
33 Perry Ave
P.O. Box 779
Attleboro, MA 02703
(617)-222-2202

8. Vacuum wand and tips from H-Square Co.

Vacuum wand	NOS	$28.14 @
Vacuum wand w/conductive connection for ESD protection		
	NOSCA	$66.00 @
Tip-modified (to fit Signetics alignment blocks)		
	T502VG(SPECIAL)	$186.00/6 ea

Supplier: H-Square Co.
1289-H Reamwood Ave
Sunnyvale, CA 94089
(408)734-2543

9. Mounting screws.

Phillips pan head machine screws		
	4-40 X 3/8	$0.02 @ 100's
	4-40 X 3/4	$0.02 @ 100's
	6-32 X 3/8	$0.03 @ 100's

Supplier: Bonneville Industry Supply Co.
45 So. 1500 W.
Orem, Utah 84058
(801) 225-7770

10. Banana Plug Jack.

H.H. Smith Type	Order #	
White 1509-101	28F1178	3/board-color your choice
Red 1509-102	35F870	3/board-color your choice
Black 1509-103	35F869	3/board-color your choice
Green 1509-104	28F1179	3/board-color your choice
Blue 1509-105	28F1180	3/board-color your choice
Yellow 1509-107	28F1182	3/board-color your choice
		$ .35 @ 3 's

Supplier: Newark Electronics.

Printed circuit board test fixtures for high-speed logic AN602

Construction Hints:

A suggested order of assembly is as follows:

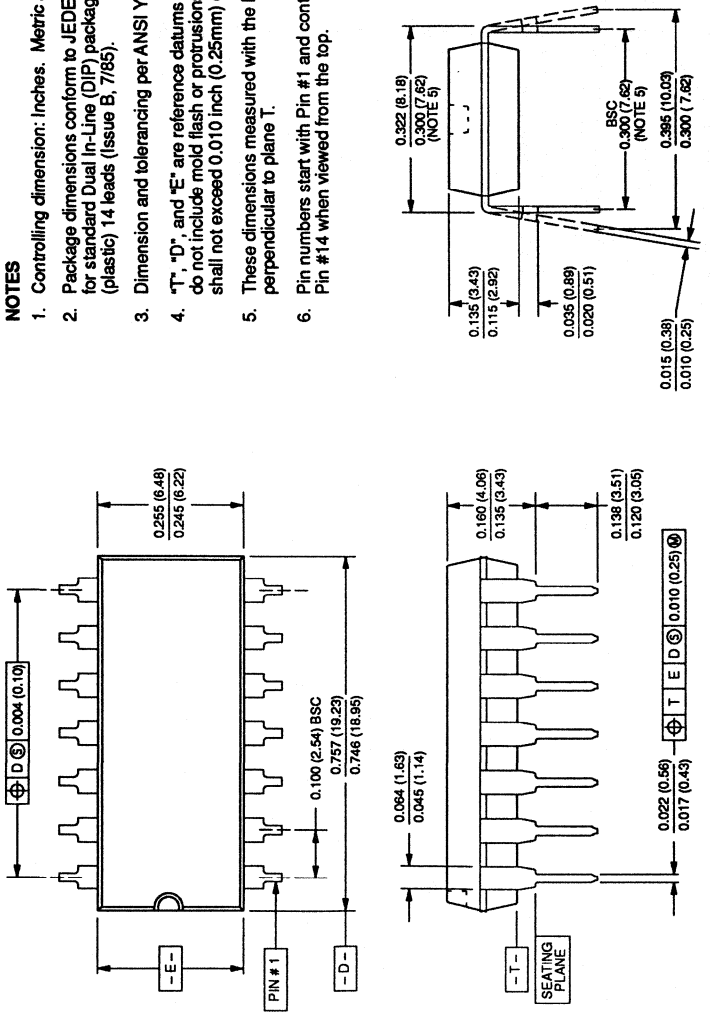
1. Install SMB Connectors. Elevate base from board .05" (this can be done with a shim or the posts can be soldered flush with the bottom side of the PC board).
2. Install Augat pin-sockets (3-S or DIP boards only, use a device inserted into the sockets on the DIP boards to hold them steady or tape over the open end of the socket with masking tape and remove after soldering).
3. Install 453 Ohm load/termination resistors (for surface mount components apply a drop of solder to one pad then reflow and mount the component, then solder the other side to its pad).
4. Install the 56.2 Ohm load/termination resistors and load caps (solder the ends on the individual lines and then the common GND connections).
5. Install banana jacks.
6. Connect V_{CC}, GND, and V_T supplies from banana jacks to board.
7. Attach alignment blocks and guides with 4-40 Phillips pan head machine screws (SMT boards only).
8. Remove all remaining flux. Keep "flux-off" or other solvent from banana jacks.

Section 7
Package Outlines

INDEX

Package outlines

14-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



NOTES

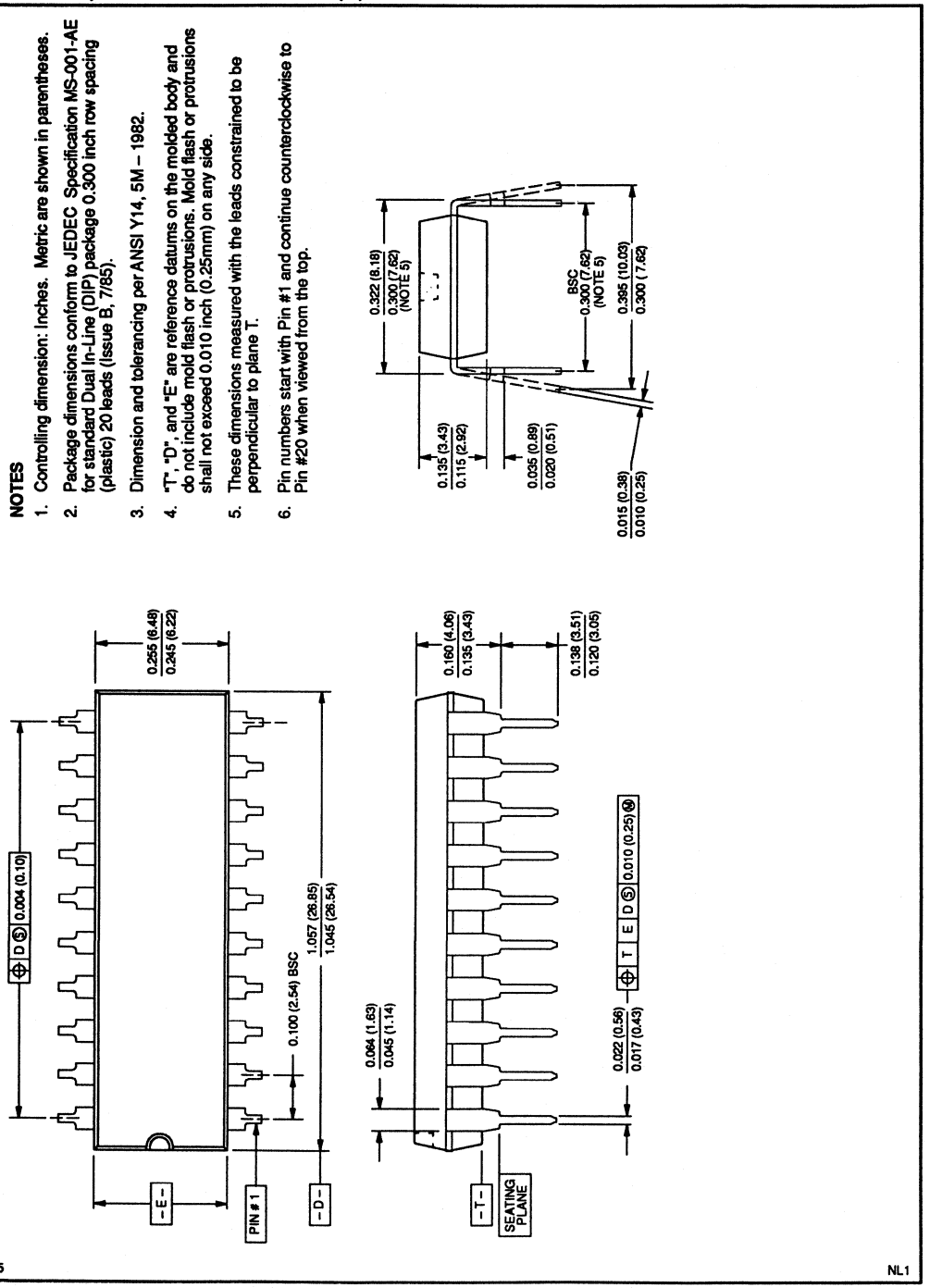
1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AC for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 14 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #14 when viewed from the top.

853-0405A 01615

NH1

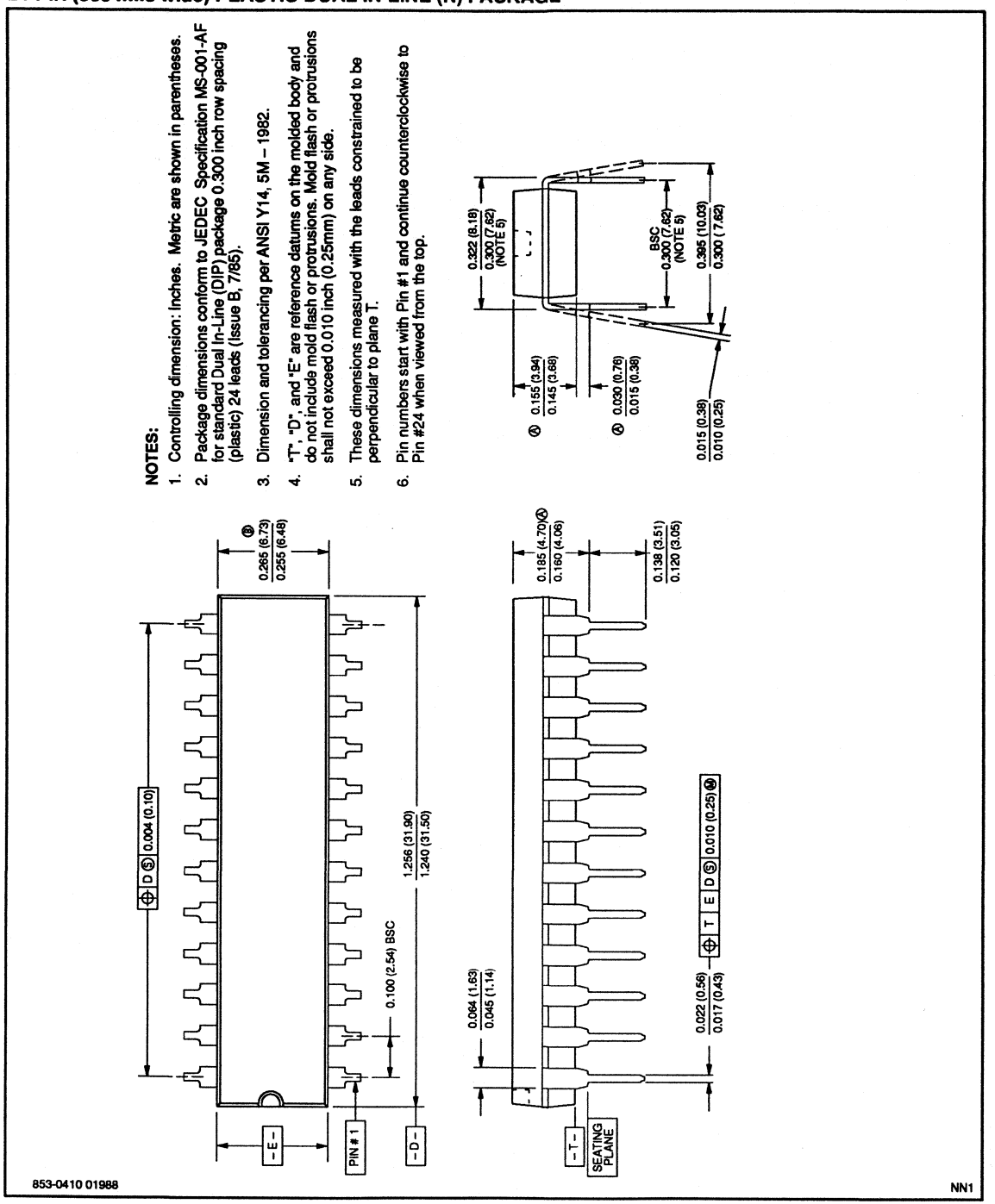
Package outlines

20-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



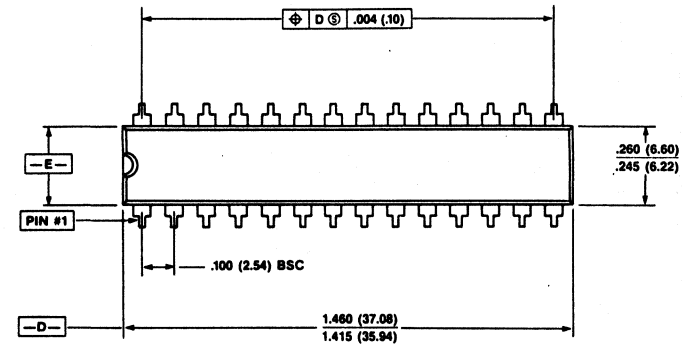
Package outlines

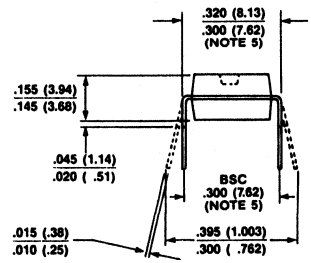
24-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



Package outlines

28-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE





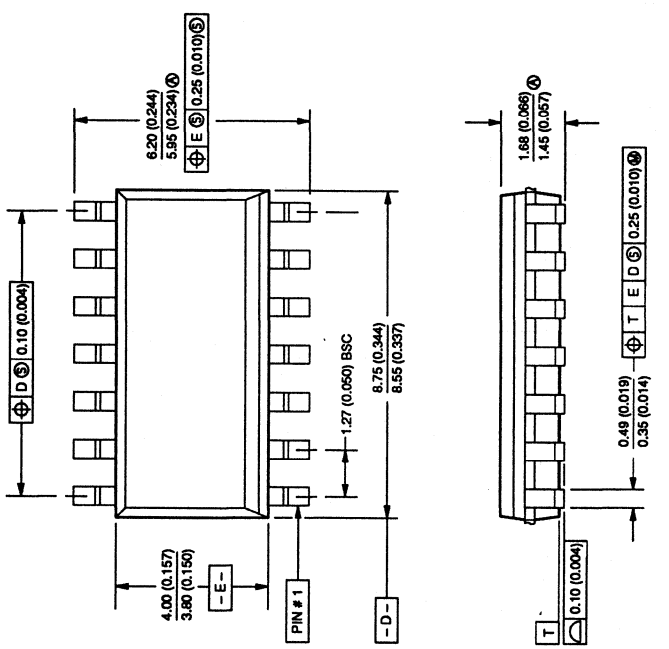
853-0864 89398

NQ1

NOTES:
1. Controlling dimensions: inches. Metric are shown in parentheses.
2. Dimensions are tolerancing per ANSI Y14.5M-1982.
3. "T", "D", and "E" are reference datums on the molded body and do not include mold-flash or protrusions which shall not exceed .010 inch (.25 mm) on any side.
4. These dimensions measured with the leads constrained to be perpendicular to plane "T".
5. Pin numbers start with #1 and continue counterclockwise to pin #28 when viewed from the top.

Package outlines

14-PIN (157 mils wide) PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D) PACKAGE



NOTES

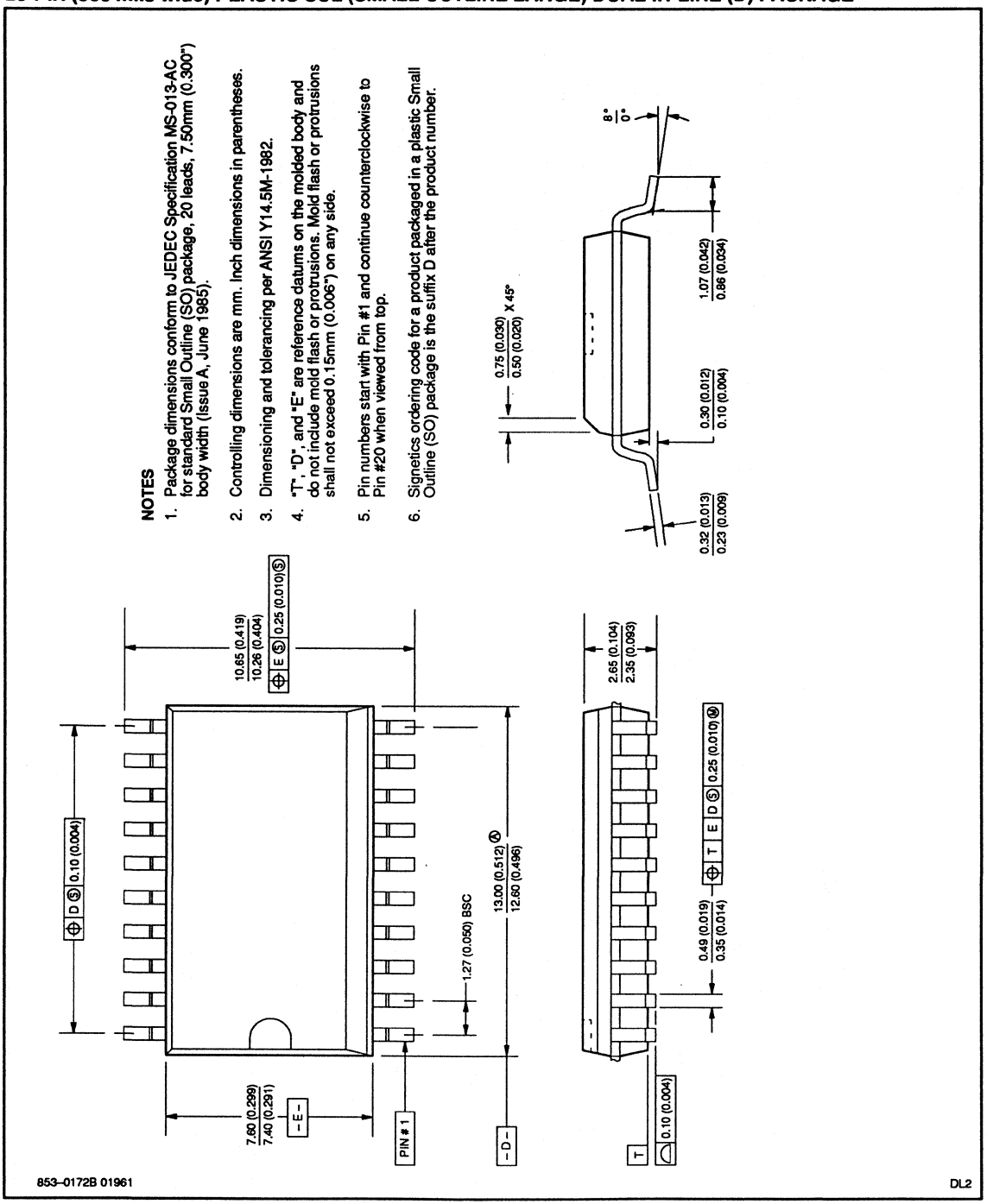
1. Package dimensions conform to JEDEC Specification MS-012-AB for standard Small Outline (SO) package, 14 leads, 3.75mm (0.150") body width (Issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (0.006") on any side.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #14 when viewed from the top.
6. Signetics ordering code for a product packages in a plastic Small Outline (SO) package is the suffix D after the product number.

853-0175B 01961

DH1

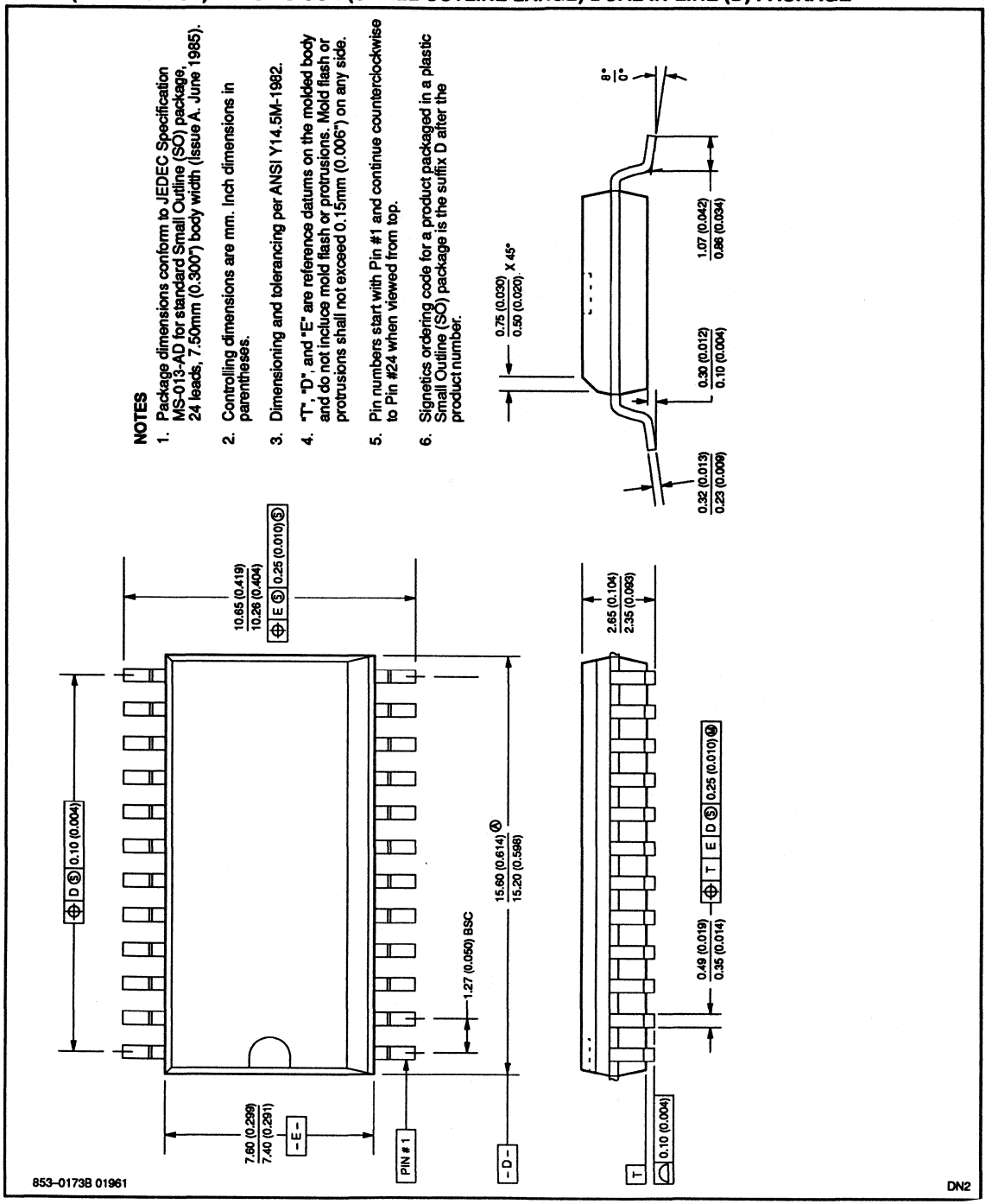
Package outlines

20-PIN (300 mils wide) PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D) PACKAGE



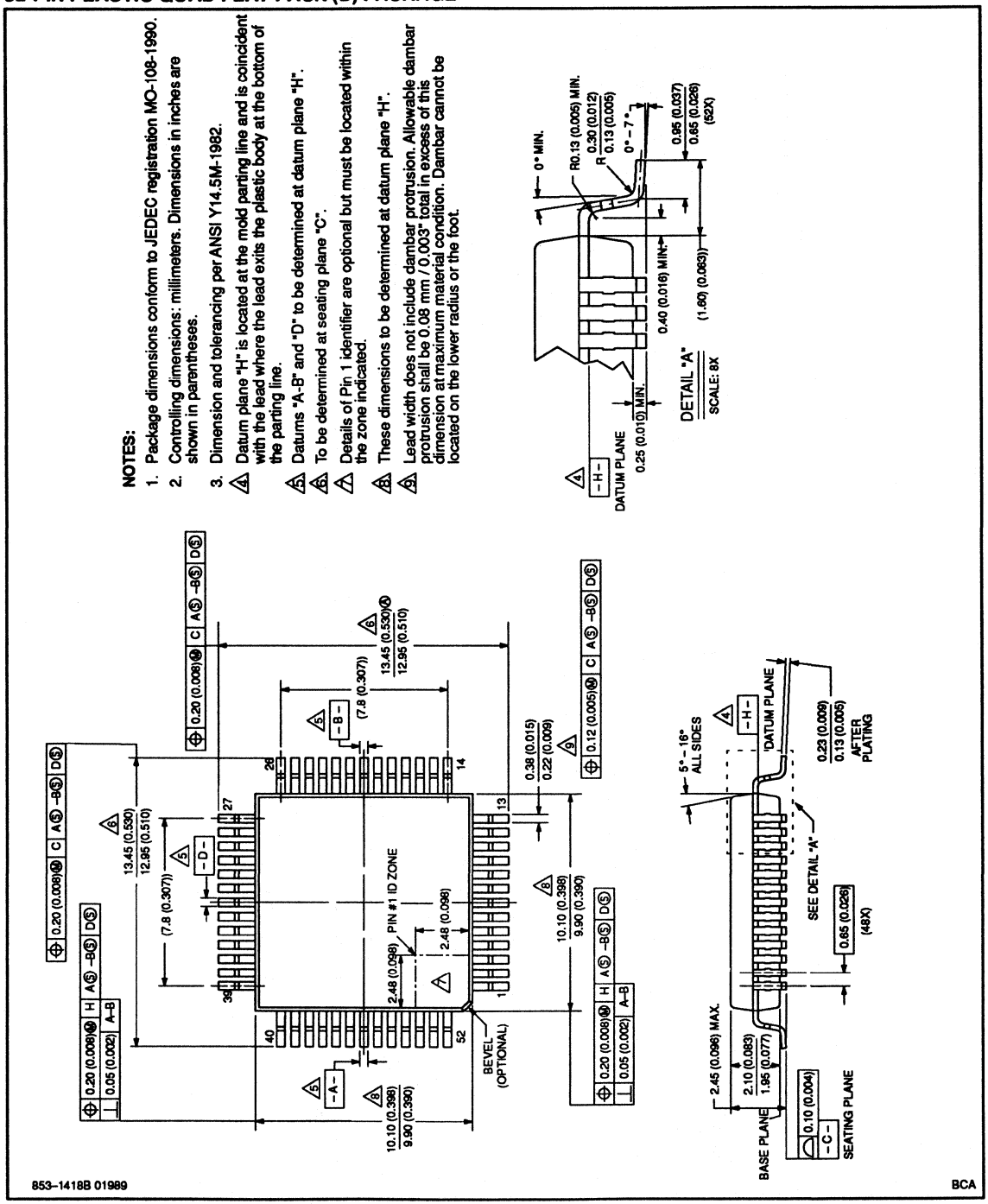
Package outlines

24-PIN (300 mils wide) PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D) PACKAGE



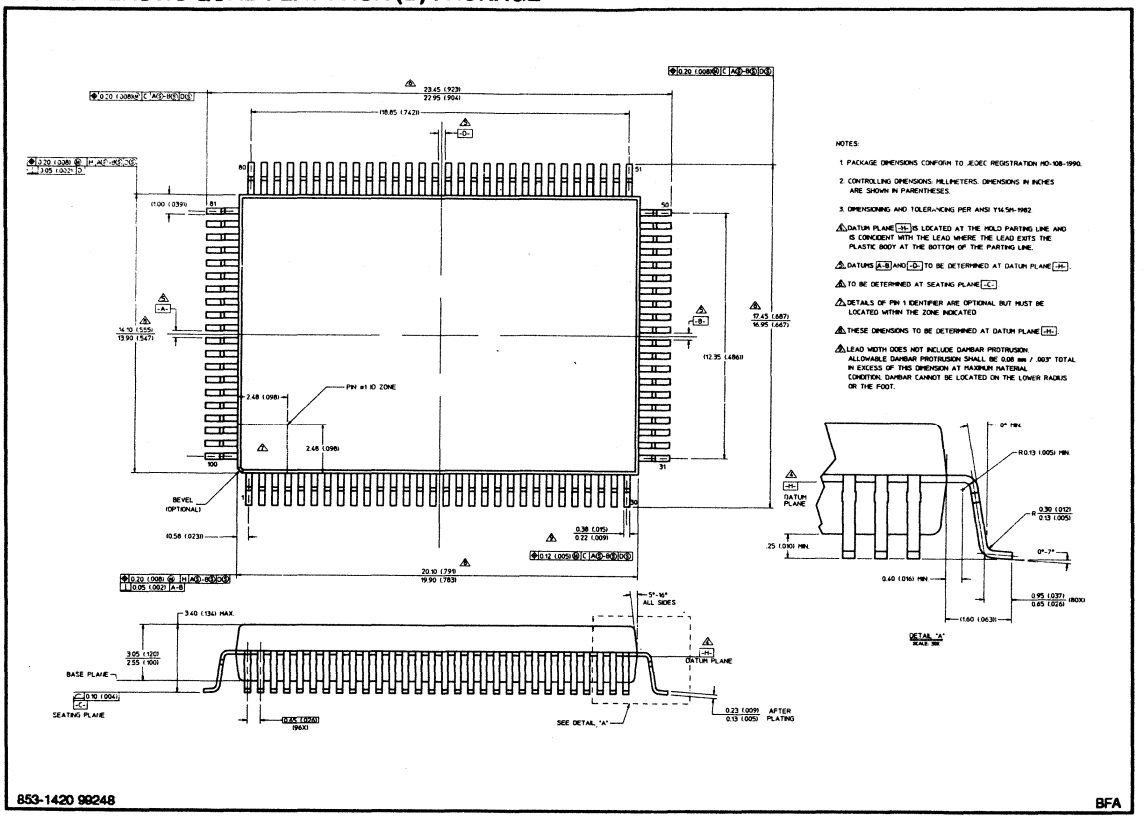
Package outlines

52-PIN PLASTIC QUAD FLAT PACK (B) PACKAGE



Package outlines

100-PIN PLASTIC QUAD FLAT PACK (B) PACKAGE



853-1420 98248 BFA

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IC06	High-speed CMOS; 74HC/HCT/HCU Logic Family
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IC07 supplement: Additional ACL data

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IC15	FAST TTL Logic Series

IC15 supplement: Additional FAST data

IC16	CMOS Integrated Circuits for Clocks and Watches
IC17	ICs for Telecom ISDN
IC18	Microprocessors and Peripherals
IC19	Data Communication Products
IC20	8051-based 8-bit Microcontrollers
IC23	Advanced BiCMOS Interface Logic

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SC01	Diodes
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SC05	Low-frequency Power Transistors and Hybrid IC Power Modules
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SC07	Small-signal Field-effect Transistors
SC08a	RF Power Bipolar Transistors
SC08b	RF Power MOS Transistors
SC09	RF Power Modules
SC10	Surface Mounted Semiconductors
SC12	Optocouplers
SC13	PowerMOS Transistors
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